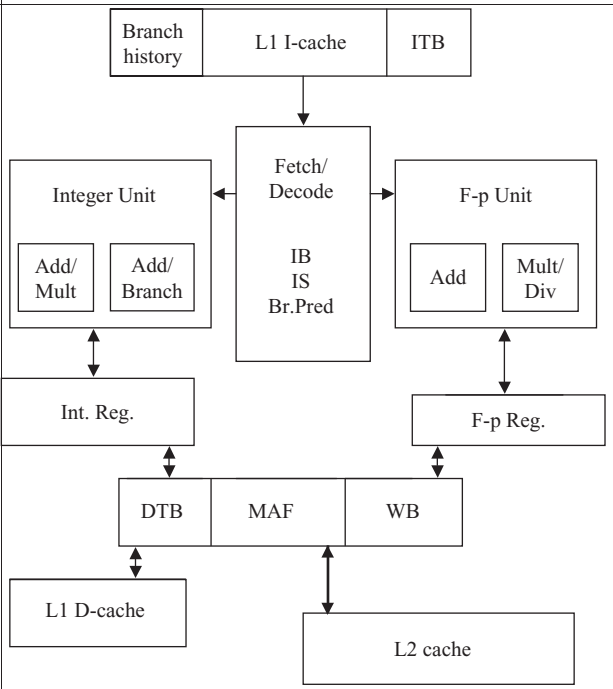


Figure 03-01.

Convert Art

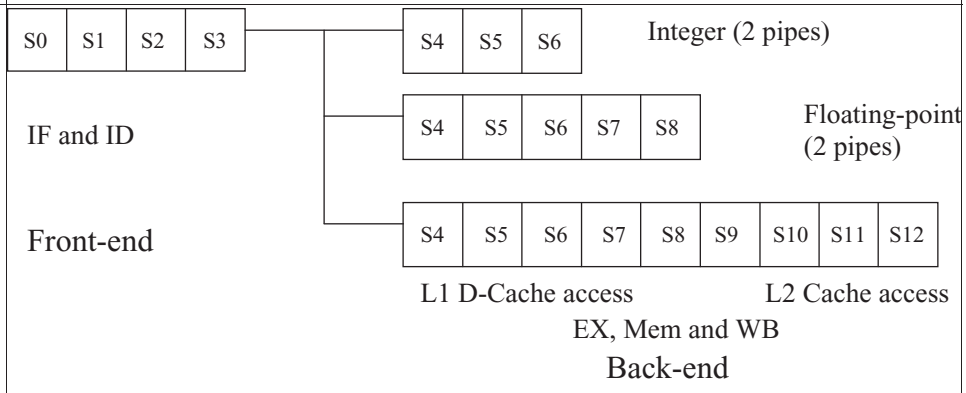
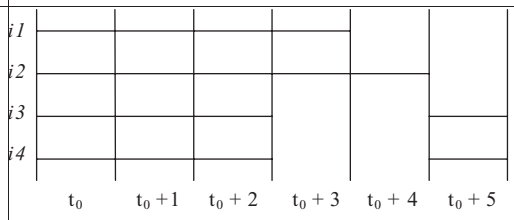


Figure 03-02.

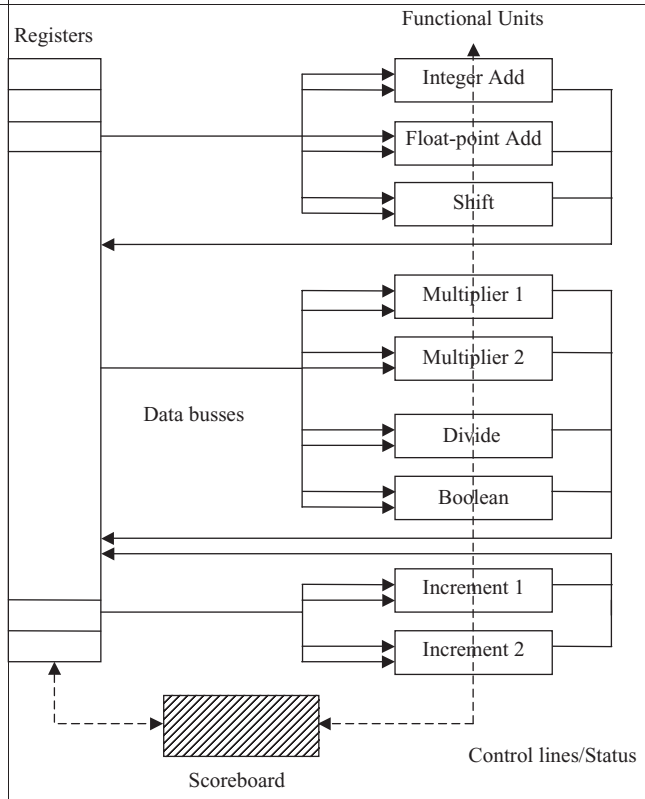
Convert Art



At time t_0 the four instructions are in stage S0.
All four are in S1 at time $t_0 + 1$ and in S2 at $t_0 + 2$. New instructions fill stages S0 and S1.
At time $t_0 + 3$ only *i1* and *i2* pass to S3. *i3* and *i4* remain in S2. No new instructions are fetched.
At time $t_0 + 4$ *i1* passes to the back-end. *i2* remains in S3; *i3* and *i4* remain in S2. No new instructions are fetched.
At time $t_0 + 5$ *i2* passes to the back-end. *i3* and *i4* pass to S3. The instructions in S1 and S0 can progress and new instructions are fetched.

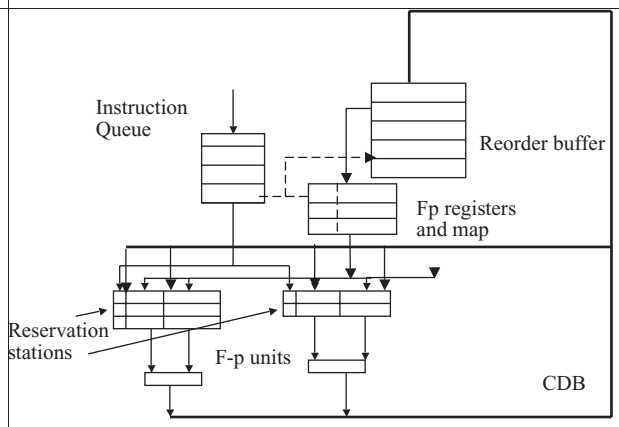
Convert Art

Figure 03-03.



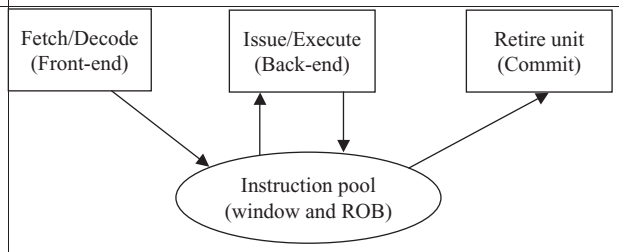
Convert Art

Figure 03-04.



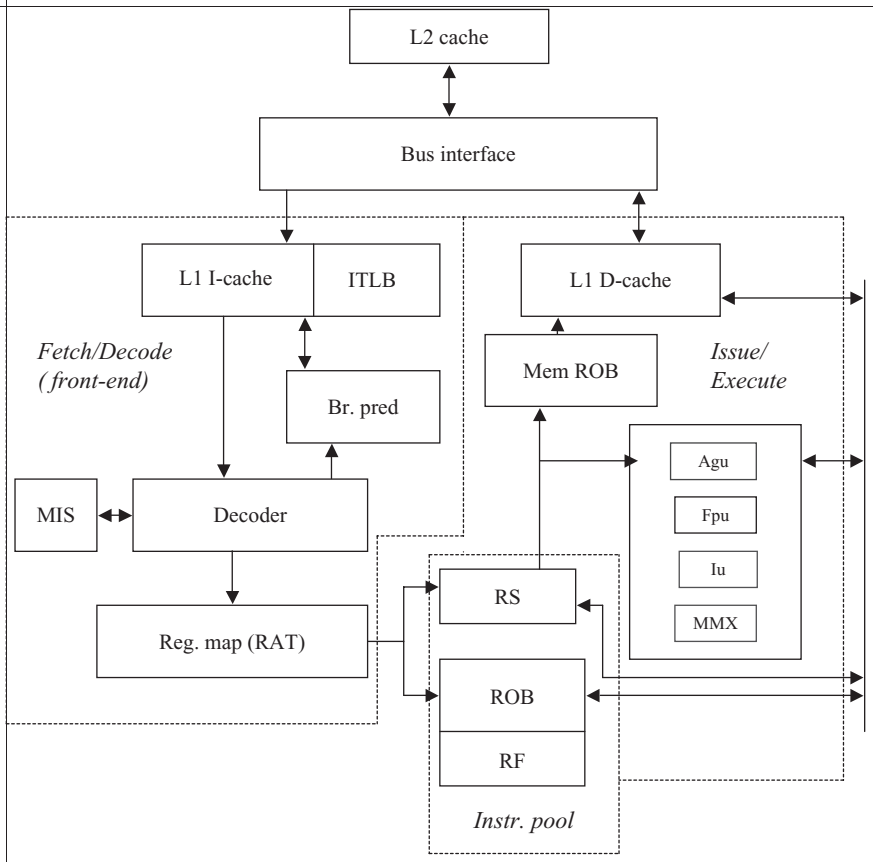
Convert Art

Figure 03-05.



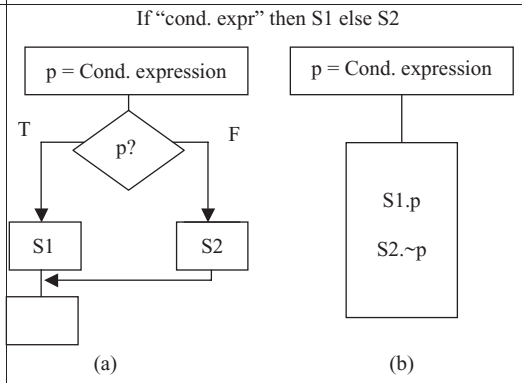
Converte Art

Figure 03-06.



Convert Art

Figure 03-07.



Convert Art

Figure 03-08.

Instruction 2 (41 bits)	Instruction 1 (41 bits)	Instruction 0 (41 bits)	Template (5 bits)

(a) A 3-instruction 128-bit bundle

Ocode 14 bits	Register 1 7 bits	Register 2 7 bits	Register 3 7 bits	Predicate 6 bits

(b) Instruction Format

Convert Art

Figure 03-09.

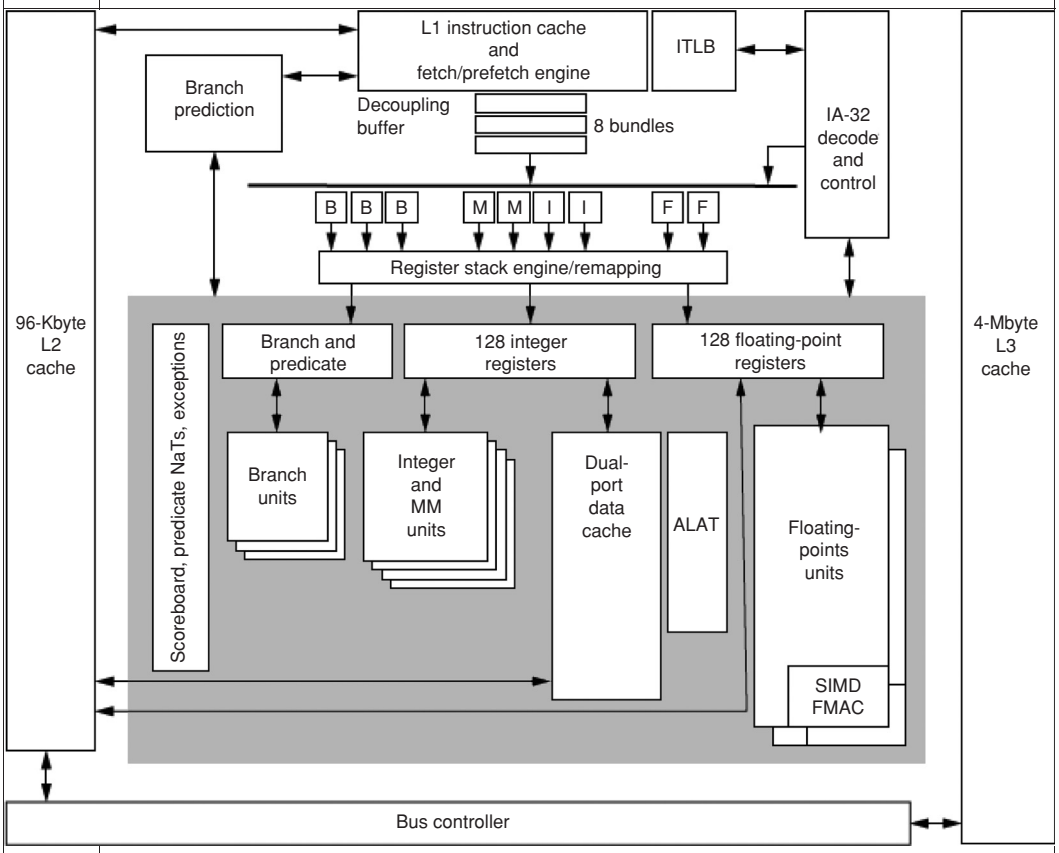
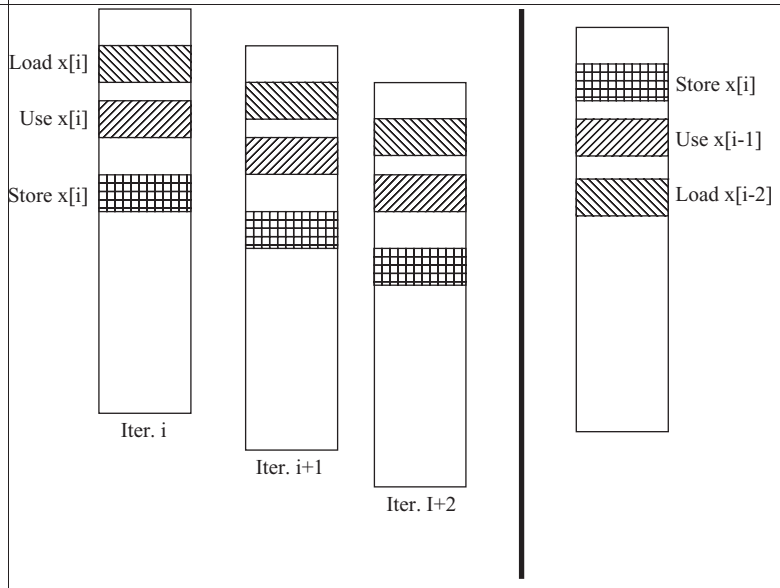


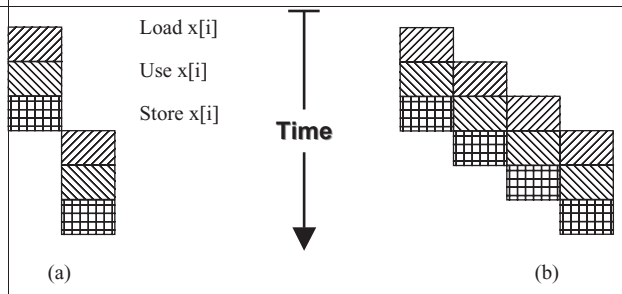
Figure 03-10.

Convert Art



Convert Art

Figure 03-11.



Convert Art

Figure 03-12.