CAMBRIDGE UNIVERSITY PRESS
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Cambridge University Press
The Edinburgh Building, Cambridge CB2 8RU, UK

Published in the United States of America by Cambridge University Press, New York

www.cambridge.org
Information on this title: www.cambridge.org/9780521857277

First published 2010
Second printing 2011

Printed in the United Kingdom at the University Press, Cambridge

A catalogue record for this publication is available from the British Library

Library of Congress Cataloging-in-Publication Data

Sarpeshkar, Rahul
Ultra low power bioelectronics : fundamentals, biomedical applications, and bio-inspired systems / Rahul Sarpeshkar.
p. cm.
ISBN 978-0-521-85727-7 (hardback)
1. Low Power Systems. 2. Biomimetics. 3. Bioelectronics. 4. Bionics. 5. Medical Electronics. 6. Synthetic Biology. 7. Systems Biology. 8. Energy Efficient Systems. I. Title.
TK7881.15.S27 2010
621.381–dc22

2009047509

ISBN 978-0-521-85727-7 Hardback

Additional resources for this publication: www.cambridge.org/9780521857277

view a diode as having a 'turn-on threshold' of 0.6 V due to the steep nature of its exponential current–voltage characteristics, it is sometimes useful to view a transistor as having an abrupt threshold voltage at which it turns on.

The 'leakage current' in a transistor that is turned off in a digital system is dominated by the transistor's subthreshold current. Such leakage current can be considerable in large digital systems. For example, 100 million transistors $\times$ 1 nA of leakage current per transistor yields 100 mA of standby leakage current. Due to the lowering of the threshold voltage of the transistor in advanced transistor processes, the absolute value of the subthreshold leakage current increases as MOS technologies progress towards ever-smaller dimensions. Subthreshold operation also occupies an increasingly larger fraction of the range of power-supply operation as transistor sizes get progressively smaller. For all of these reasons, there has been a great renewal of interest in the subthreshold regime of operation. Subthreshold operation in both analog and digital circuits has almost become a necessity.

The maximal frequency of operation possible in diffusion-current-determined subthreshold operation scales inversely with the square of the transistor's channel length. In contrast, the maximal speed of velocity-saturated above-threshold operation only scales inversely with the channel length. Thus, subthreshold operation is rapidly allowing faster speeds of operation and may no longer be viewed as a 'slow regime' of operation of the transistor. For example, 1 GHz analog preamplifiers with all-subthreshold operation can now be built in a 0.18 μm process and digital circuits can be made to operate at such speeds as well.

The subthreshold region of operation is a region where the bandwidth available per ampere of current consumed in the transistor is maximal. The power-supply voltage needed for subthreshold operation is also minimal since the saturation voltage of a transistor in subthreshold is only 0.1 V. Due to the high bandwidth-per-ampere ratio and the ability to use small power-supply voltages, the bandwidth per watt of power consumed in the transistor is maximized in its subthreshold regime. Consequently, subthreshold operation is the most power-efficient regime of operation in a transistor.

For all these reasons, this book focuses heavily on the use of subthreshold circuits for ultra-low-power electronic design in the analog and the digital domains. In the subthreshold region of operation, often also referred to as the weak-inversion region of operation, it is important to ensure that systems are robust to transistor mismatch, power-supply-voltage noise, and temperature variations. Hence, circuit biasing and feedback techniques for ensuring robustness are important. We shall discuss them in various contexts in the book, but particularly in Chapter 19, where we discuss the design of ultra-low-power biomedical system chips for implantable applications, and in Chapter 21 on ultra-low-power digital design. Furthermore, the subthreshold regime is characterized by relatively high levels of noise, since there are few electrons per unit time to average over. Thus, throughout the book, we shall discuss device noise, how to mitigate it, how to analyze it, how to design around it, and, in some cases, how to even exploit it.

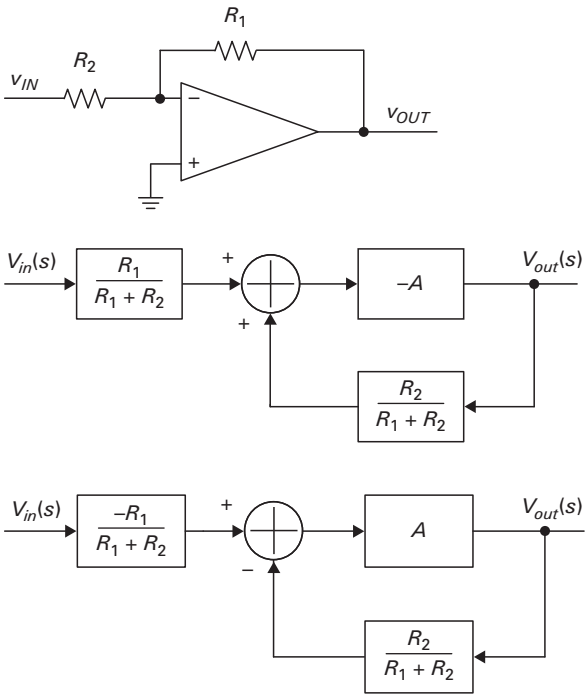

Figure 2.4. Non-inverting amplifier circuit (top) and associated block diagrams before (middle) and after (bottom) simplification into the standard negative-feedback form.

From Figure 2.2, we can also quickly derive that the error transfer function $\varepsilon(s)/V_{in}(s)$ is given by

$$\frac{\varepsilon(s)}{V_{in}(s)} = \frac{1}{1 + a(s)f(s)} \tag{2.4}$$

and is small if $|a(s)f(s)| \gg 1$. In fact, it is the fundamental principle of Equation (2.4) that leads to the rule of thumb that $v_- \approx v_+$ in an operational amplifier circuit. If the error voltage $v_+ - v_-$ builds in magnitude, a negative-feedback loop with a sufficiently high loop gain, which is due to sufficiently high operational-amplifier gain, will attenuate this error voltage until it is nearly zero. Figure 2.4 shows an inverting amplifier configuration. Simple manipulations of the block diagram describing its operation convert it to the standard feedback block diagram as shown. The ideal closed-loop transfer function between the input and output if the loop gain or equivalently the operational-amplifier gain is sufficiently large is then given by

$$\frac{V_{out}}{V_{in}} = \frac{-R_1}{R_1 + R_2} \times \frac{R_1 + R_2}{R_2} = \frac{-R_1}{R_2} \tag{2.5}$$

The non-inverting amplifier of Figure 2.3 and the inverting amplifier of Figure 2.4 both have the same value of loop transmission $a(s)f(s)$ but different

from gate to bulk to be C_{ox}. The figure also reminds us that the reason for the charge-diode-clamp behavior in strong inversion is the presence of a strong negative-feedback loop between electron concentration and surface potential.

3.8 Quantitative discussion of the MOSFET

Figure 3.13 shows a half MOSFET, i.e., an n+ region bordering a MOSCAP. The n+ region now presents an alternate region of low energy for electrons to reside and also provides an abundant supply of electrons. Increasing the potential v_{CB} of the n+ region with respect to the bulk lowers the energy of the n+ region with respect to the bulk. It also decreases the concentration of minority-carrier electrons in the bulk region near the n+ border by $\exp(-v_{CB}/\phi_t)$ just as in a reverse-biased diode. Across any diode-like junction, a balance between drift currents (due to electric fields in depletion regions of the diode) and diffusion currents (due to electron concentration differences across the diode junction) leads to an equilibrium minority carrier concentration at the edge of the junction that is exponentially dependent on the voltage across the junction. In effect, a positive value of v_{CB} functions to contribute a reverse-bias voltage to the diode-like element of Figure 3.4, which in a half MOSFET only exists on one side. The lack of current flow in the half MOSFET means that the electron concentration and surface potential are the same all along the horizontal x dimension of the channel at any given value of y. The variation in electron concentration $n_0(y)$ along the vertical y dimension is still described by the exponential relationship of Equation (3.7) in the MOSCAP in a long-channel scenario except that we now have an extra factor of $\exp(-v_{CB}/\phi_t)$ in the equation:

$$n_0(y) = N_A e^{-v_{CB}/\phi_t} e^{-2\phi_F/\phi_t} e^{+\psi(y)/\phi_t} \tag{3.15}$$

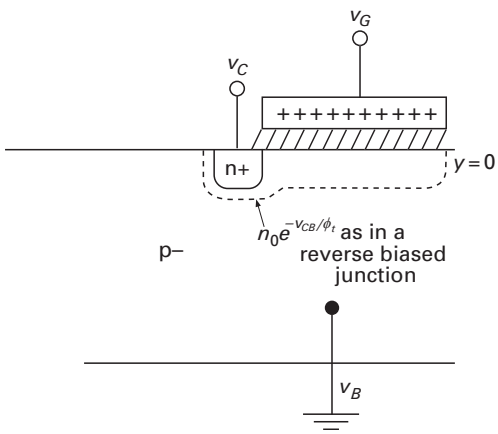

Figure 3.13. MOSCAP + 1 control terminal.

4 MOS device physics: practical treatment

Although this may seem a paradox, all exact science is dominated by the idea of approximation.

Bertrand Russell

In Chapter 3, we discussed an intuitive model to describe transistor operation shown in Figure 3.4. We will now use this intuitive model to simplify Equation (3.23) into more practical and insightful forms in subthreshold and above-threshold operation. To do so, we will use three approximations listed below.

1. **The κ approximation.** We approximate $\gamma\sqrt{\psi_S}$ by a constant term $\gamma\sqrt{\psi_{se}}$ around an operating point ψ_{se} plus a Taylor-series linear term $\left(\gamma/2\sqrt{\psi_{se}}\right)(\psi_S - \psi_{se})$ to describe deviations from the operating point. This approximation is equivalent to modeling the distributed nonlinear depletion capacitance C_{dep}, shown in Figure 3.4 as a linear capacitance with some fixed value around a given ψ_{se}. The surface potential ψ_s varies with x in above-threshold operation, such that C_{dep} varies along the channel in Figure 3.4. We ignore this variation and assume one value for C_{dep} throughout the channel given by $\gamma C_{ox}/(2\sqrt{\psi_{se}})$ from Equation (3.11). The chosen operating point ψ_{se} is usually at the subthreshold to above-threshold transition where we have good knowledge of the surface potential and, in addition, is at the source channel end in source-referenced models. The value of $\kappa = C_{ox}/\left(C_{ox} + C_{dep}\right)$ is always between 0 and 1 and given by a capacitive-divider ratio. The κ approximation is useful in weak inversion and strong inversion. **The parameter $\kappa = 1/n$ by definition, where n is termed the subthreshold slope coefficient in some texts**.
2. **The Taylor-series square-root approximation.** In weak inversion, we assume that the $\phi_t \exp(\ldots)$ term in $\gamma C_{ox}\sqrt{(\psi_S + \phi_t \exp((\psi_S - 2\phi_F - v_{CB})/\phi_t))}$, an expression that describes the total charge at the source channel end or drain channel end, is much smaller than the ψ_S term in the expression. Therefore, we use a Taylor-series approximation for the square root again to evaluate the total charge in the expression. This approximation is useful in weak inversion only. Note that $v_{CB} = v_{SB}$ at the source end and $v_{CB} = v_{DB}$ at the drain end.
3. **The diode-clamp approximation.** In strong inversion, we will assume that the diode-like element of Figure 3.4 clamps the surface potential at the source end of the channel to $(2\phi_F + 6\phi_t) + v_{SB} = \phi_0^s + v_{SB}$ due to the operation of a strong negative-feedback loop. The surface potential at the drain end of the channel

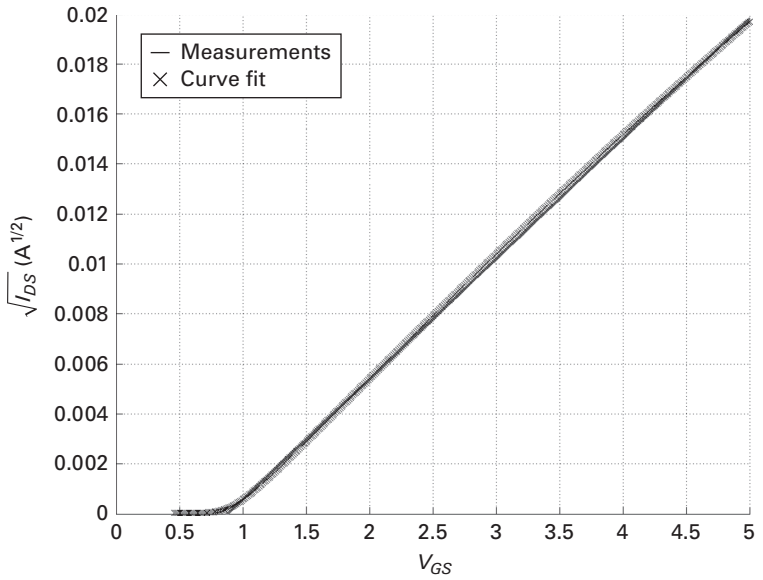

Figure 4.8. Experimentally measured square-root current characteristics in the above-threshold regime.

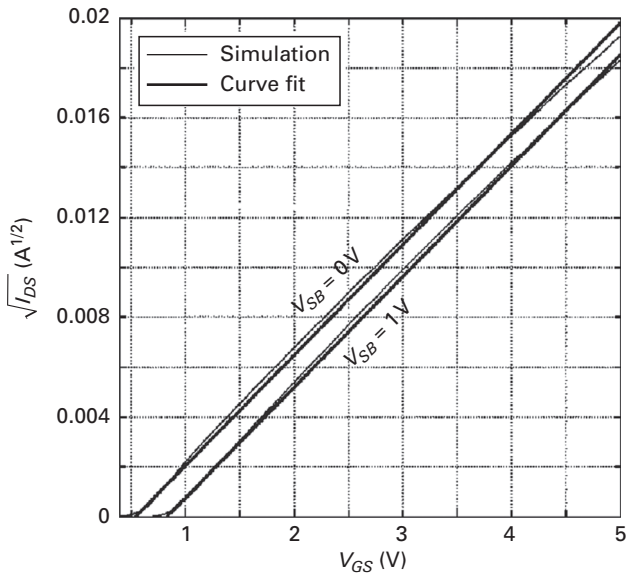

Figure 4.9. Simulated body effect in the above-threshold regime.

The source-referenced model is described by

$$i_{DS} = I_{0S} e^{\kappa_S v_{GS}/\phi_t}(1 - e^{-v_{DS}/\phi_t}) \tag{5.5}$$

where

$$\begin{aligned} I_{0S} &= \mu C_{ox} \phi_t^2 \frac{W}{L}\left(\frac{1-\kappa_{sa}}{\kappa_{sa}}\right) e^{-\kappa_S V_{TS}/\phi_t} \\ \kappa_S &= \frac{1}{1 + \dfrac{\gamma}{2\sqrt{\phi_0 + V_{SB}}}} = \frac{1}{n_S} \\ V_{TS} &= V_{T0} + \gamma\left(\sqrt{(\phi_0 + V_{SB})} - \sqrt{\phi_0}\right) \end{aligned} \tag{5.6}$$

By differentiating Equation (5.5) with respect to v_{GS}, we can see that

$$g_m = \frac{\kappa_S I_{DS}}{\phi_t} \tag{5.7}$$

Thus, the g_m of a subthreshold MOS transistor is very similar to the g_m of a bipolar transistor, I_C/ϕ_t, where I_C is the collector current except for the κ_S term.

We evaluate g_{mb} from Equations (5.5) and (5.6) to be

$$\begin{aligned} g_{mb} &= \frac{\partial I_{0S}}{\partial V_{TS}} \times \frac{\partial V_{TS}}{\partial v_{BS}} = \left(-\frac{\kappa_S}{\phi_t} I_{DS}\right) \times \left(-\frac{1-\kappa_S}{\kappa_S}\right) \\ &= \frac{(1-\kappa_S) I_{DS}}{\phi_t} \end{aligned} \tag{5.8}$$

It is interesting to derive the same result from a body-referenced viewpoint as well. Equation (5.3) can be rewritten as follows:

$$\begin{aligned} i_{DS} &= I_0 e^{(\kappa_0 v_{GB} - v_{SB})/\phi_t}(1 - e^{-v_{DS}/\phi_t}) \\ &= I_0 e^{(\kappa_0 (v_{GB} - v_{SB}) - (1-\kappa_0) v_{SB})/\phi_t}(1 - e^{-v_{DS}/\phi_t}) \\ &= I_0 e^{\kappa_0 v_{GS}/\phi_t} e^{(1-\kappa_0) v_{BS}/\phi_t}(1 - e^{-v_{DS}/\phi_t}) \end{aligned} \tag{5.9}$$

from which we can see that $g_m = \kappa_0 I_{DS}/\phi_t$ and $g_{mb} = (1-\kappa_0) I_{DS}/\phi_t$.

Equation (5.9) highlights the symmetry of the gate and bulk terminals in controlling the transistor. In fact, an even simpler way to derive g_{mb} is to note, from the discussion in Chapter 4, that the transistor current is given by

$$i_{DS} = (\ldots) e^{\psi_{sa}/\phi_t}\left(1 - e^{-v_{DS}/\phi_t}\right) \tag{5.10}$$

where the $(\ldots)$ refers to terms independent of v_{SB}. Then, from the capacitive divider relationship obvious from Figure 3.4,

$$\begin{aligned} g_{mb} &= \frac{\partial i_{DS}}{\partial v_{BS}} = \frac{I_{DS}}{\phi_t}\frac{\partial \psi_{sa}}{\partial v_{SB}} \\ &= \frac{I_{DS}}{\phi_t}\left(\frac{C_{dep}}{C_{dep} + C_{ox}}\right) \\ &= \frac{I_{DS}}{\phi_t}(1-\kappa) \end{aligned} \tag{5.11}$$

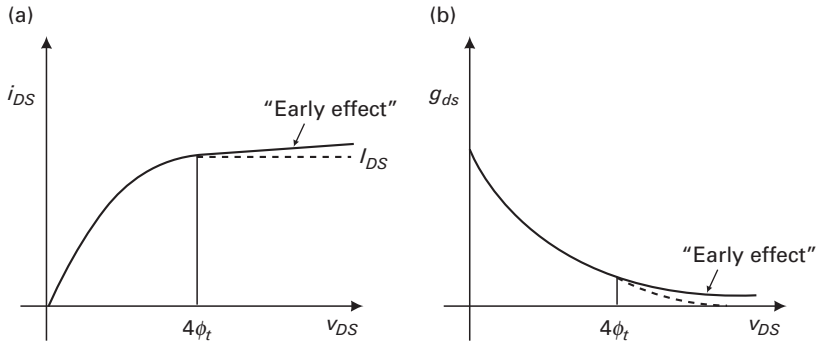

Figure 5.1a, b. Early voltage curves in the subthreshold regime.

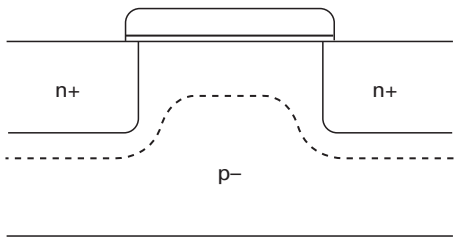

Figure 5.2. Depletion regions at the source and drain illustrating the origin of the Early effect.

Equations (5.7) and (5.11) illustrate that both the gate and bulk behave like good control terminals with a gate and bulk transconductance respectively. In Chapter 12, we will exploit circuits that use the bulk (the well terminal in a pFET) as a legitimate control terminal instead of merely tying it to the power supply, as is often done.

By differentiating Equation (5.5), we can derive that,

$$\frac{\partial i_{DS}}{\partial v_{DS}} = \frac{I_{0S} e^{\kappa V_{GS}/\phi_t} e^{-V_{DS}/\phi_t}}{\phi_t}$$
$$g_{ds} = \frac{I_{DSAT}}{\phi_t} e^{-V_{DS}/\phi_t} \tag{5.12}$$

Equation (5.12) predicts that g_{ds} asymptotically approaches zero after $V_{DS} \geq 4\phi_t$. However, in practice, an effect called the Early effect causes g_{ds} to remain finite after the saturation voltage as illustrated by the $i_{DS} - v_{DS}$ curve and $g_{ds} - v_{DS}$ curve of Figure 5.1.

Figure 5.2 shows that the length l_p, the sum of the depletion region length at the source end and drain end of the channel, reduces the effective channel length of the transistor from L to $L - l_p$: The edges of the depletion regions at the source end and drain end of the channel are the locations where the boundary conditions for the surface potential and charge are valid, and between which integration of the

The relations of Equations (5.34) and (5.37) along with Equation (5.30) can be used to derive capacitance results for each V_{DS} operating point in strong inversion. The derivations are simple mathematical exercises in differentiation and integration. Since all capacitances in Equations (5.34) and (5.37) are expressed in terms of Q_I^{TOT}, it is extremely useful to evaluate it explicitly from simple integration of $Q_I(x)$ in Equation (5.32) to obtain

$$\begin{aligned} Q_I^{TOT} &= W\int_0^L Q_I(x)dx \\ Q_I^{TOT} &= \frac{2}{3}WL\left[\frac{Q_{I0}^2 + Q_{IL}^2 + Q_{I0}Q_{IL}}{(Q_{I0} + Q_{IL})}\right] \\ Q_I^{TOT} &= \frac{2}{3}WL\left[(Q_{I0} + Q_{IL}) - \frac{Q_{I0}Q_{IL}}{(Q_{I0} + Q_{IL})}\right] \end{aligned} \tag{5.38}$$

If we define

$$\eta = 1 - \frac{V_{DS}}{V_{DSAT}} = \frac{Q_{IL}}{Q_{I0}} \tag{5.39}$$

such that η goes from 1 to 0 as V_{DS} goes from 0 to V_{DSAT}, then it can be shown that

$$\begin{aligned} C_{gs} &= \frac{2}{3}WLC_{ox}\left(\frac{1+2\eta}{(1+\eta)^2}\right), \quad C_{gd} = \frac{2}{3}WLC_{ox}\left(\frac{\eta^2+2\eta}{(1+\eta)^2}\right) \\ C_{bs} &= \left(\frac{1-\kappa_S}{\kappa_S}\right)C_{gs}, \quad C_{bd} = \left(\frac{1-\kappa_S}{\kappa_S}\right)C_{gd} \\ C_{gb} &= WLC_{ox}\left(\frac{1-\kappa_S}{3}\right)\left(\frac{1-\eta}{1+\eta}\right)^2 = (1-\kappa_S)\left(C_{ox}WL - \left(C_{gs}+C_{gd}\right)\right) \end{aligned} \tag{5.40}$$

with

$$i_{DS} = i_{DSAT}\left(1-\eta^2\right) \tag{5.41}$$

Figure 5.7 plots Equation (5.40) and reveals how the various small-signal capacitances in the MOS transistor change as V_{DS} changes. The most significant point to note is that C_{gs} changes from 1/2 to 2/3 of WLC_{ox} while C_{gd} changes from 1/2 to 0 of WLC_{ox} as the transistor moves from the linear to saturation regime. The next significant point to note is that C_{bs} and C_{bd} are proportional to C_{gs} and C_{gd} with the same proportionality factor of $g_{mb}/g_m = (1-\kappa_S)/\kappa_S$. Finally, C_{gb} rises from 0 to a small but finite value as we transition from the linear to saturation regime in the transistor. Figure 5.8 (a) shows the 'capacitance diamond', the five capacitances incorporated into a small-signal equivalent circuit. Figure 5.8 (b) shows the capacitances, conductance, and transconductances of the transistor all in one complete small-signal model. Often, v_B is a fixed voltage. Then, C_{gb}, C_{bs}, and C_{bd} all form grounded capacitances, and C_{gs} and C_{gd} are analogous to C_π and C_μ in bipolar transistors, respectively.

It is interesting to derive the general results of Equation (5.40) for certain special cases that provide insight, easily obscured by algebra. If the transistor is saturated,

The capacitance C_{gd} is zero in the saturation regime since $Q_{IL} = 0$, such that changes in v_D do not affect $Q_I(x)$ or any other charges in the transistor. In practice, slight changes in the length of the transistor with changes in v_D (Early effect changes in the length) do reduce the total inversion charge such that C_{gd} is non zero.

If the transistor is in its linear regime with $V_{DS} = 0$, the square-root distribution for $Q_I(x)$ changes to a flat distribution with $Q_{I0} = Q_{IL}$. An infinitesimally small change in charge at the source end or at the drain end caused by a Δv_S or Δv_D respectively will result in the flat distribution $Q_I(x)$ acquiring a small triangular increase in area due to the change in Q_{I0} with Q_{IL} fixed or vice versa. Since the area of a triangle is (1/2) base $\times$ height, only half of the charge increase at the source end or drain end gets integrated into the total charge increase in the channel. Thus, we can show by a similar derivation as in Equation (5.42) that, when $V_{DS} = 0$,

$$C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox} \tag{5.43}$$

The capacitances C_{bs} and C_{bd} remain proportional to C_{gs} and C_{gd} with $(1-\kappa_S)/\kappa_S$ as the constant of proportionality as C_{gs} and C_{gd} vary with V_{DS}.

The capacitance C_{gb} may be understood intuitively as follows. An increase in v_B results in no boundary-condition change in the surface potential at the diode-clamped source end of the channel and thus no change in the gate charge at this end. It does however result in a decrease in the magnitude of the bulk charge at the source end due to the falling voltage difference across C_{dep}. There is then a concomitant increase in the magnitude of the inversion charge at the source end to preserve charge balance. The increase in inversion charge at the source end results in an increase in inversion charge throughout the channel due to the drift generators in the channel. At the drain end of the channel, an increase in v_B increases the surface potential via a capacitive-divider mechanism if and only if the drain end is in saturation since the diode-like element at that end is then off. In general, v_B increases will attempt to increase the surface potential via a capacitive-divider mechanism throughout the channel. However, the increase in inversion charge due to the v_B increase at the source (and/or drain end of the channel if it is not in saturation) reduces the surface potential, thus attenuating the capacitive-divider increase via a negative-feedback loop. The loop effectively operates via the diode clamps at the boundary ends of the channel and propagates via the drift generators into the interior of the channel. The net effect of the v_B increase is then to leave the surface potential and gate charge unaffected at the source end of the channel and increase the surface potential in the interior of the channel slightly with stronger increases towards the drain end of the channel and a maximal increase at the drain end after it enters saturation. The total gate charge is reduced due to falling voltages across the C_{ox} capacitances when v_B is increased, thus making C_{gb} positive. The capacitance C_{gb} is zero if and only if $V_{DS} = 0$, because, in this case, the increase in inversion charge at the boundary ends of the channel does not alter the flat-and-constant surface potential in the channel, keeping the

transitions gradually in a 'bird's-beak-like' fashion from a thick-oxide overhanging region to a thin-oxide channel region.

The actual capacitances of the transistor are composed of a portion due to intrinsic capacitances and a portion due to extrinsic capacitances. If all intrinsic portions are subscripted with an i and all extrinsic portions are subscripted with an e, we get

$$\begin{aligned} C_{gs} &= C_{gsi} + C_{gse} \\ C_{gd} &= C_{gdi} + C_{gde} \\ C_{bs} &= C_{bsi} + C_{bse} \\ C_{bd} &= C_{bdi} + C_{bde} \\ C_{gb} &= C_{gbi} + C_{gbe} \end{aligned} \tag{5.47}$$

In addition to these capacitances, a well-to-substrate depletion capacitance, C_{bbe}, is present in the transistor. This capacitance is important in circuits where the well voltage changes, e.g., when the well is used as an input. The extrinsic capacitances C_{bse}, C_{bde}, C_{gbe}, and C_{bbe} are nonlinear depletion capacitances whose values change with voltage, typically like an inverse-square-root function in abrupt junctions.

5.5 Small-signal capacitance models in weak inversion

In weak inversion, to first order, the bulk charge and gate charge are equal in magnitude and the inversion charge is zero. The source and drain terminal voltages have no effect on the surface potential and thus no effect on the gate charge or bulk charge. Thus, C_{gsi}, C_{gdi}, C_{bsi}, and C_{bdi} are zero. The only intrinsic capacitance that is significant in weak inversion is

$$\begin{aligned} C_{gbi} &= \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} WL \\ &= \frac{C_{ox}C_{ox}\left(\dfrac{1-\kappa_S}{\kappa_S}\right)}{C_{ox} + C_{ox}\left(\dfrac{1-\kappa_S}{\kappa_S}\right)} WL \\ C_{gbi} &= C_{ox}(1-\kappa_S)WL \end{aligned} \tag{5.48}$$

The extrinsic capacitances in weak inversion are all identical to those in strong inversion if the voltage dependencies of these capacitances are taken into account. Thus, the capacitances in weak inversion are given by

$$\begin{aligned} C_{gs} &= C_{gse}, \quad C_{gd} = C_{gde} \\ C_{bs} &= C_{bse}, \quad C_{bd} = C_{bde} \\ C_{gb} &= C_{ox}(1-\kappa_S)WL + C_{gbe} \end{aligned} \tag{5.49}$$

The overall small-signal circuit in weak inversion is identical to that depicted in Figure 5.8 for strong inversion except that the values of the elements in the circuit are those corresponding to weak inversion.

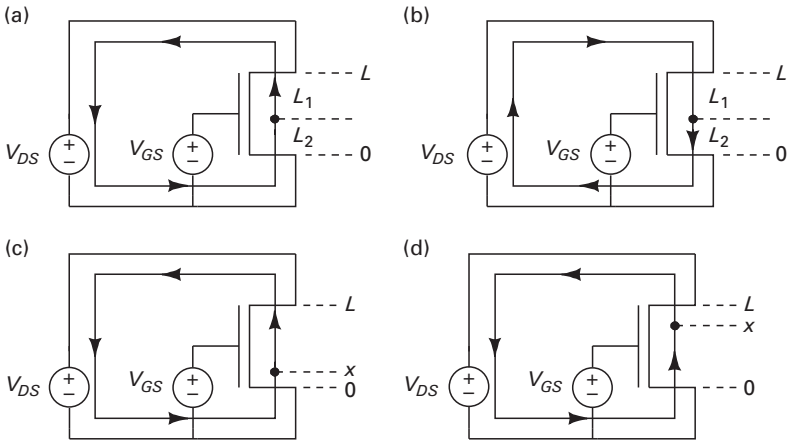

Figure 7.6a, b, c, d. The total distance that an electron must diffuse before it completes a loop and return to its starting point is independent of the sense of the loop (parts (a) and (b)). Parts (c) and (d) show that it is also independent of the location of the starting point.

Thermally generated diffusion currents exhibit shot noise because the variance in the round-trip clockwise or anticlockwise circuit travel times is well modeled by a random Poisson process. Larger temperatures, which cause higher thermal velocities, and smaller mean free times between collisions yield a larger value for the diffusion constant and larger diffusion currents. If L is the effective channel length between the edge of the source depletion region and the edge of the drain depletion region, the transit time $\tau = L^2/2D_n$ where D_n is the diffusion constant for electrons in silicon. If we assume that the depletion-region travel times and voltage-source travel times are negligible, a good approximation in long-channel transistors, the transit time is a measure of the average time taken by an electron in the channel to complete a round-trip clockwise or anticlockwise journey through the full circuit and return to its starting point. Note also that, in our method of accounting for Poisson events, a full circuit must be completed for the external voltage source to register an electronic current. Incomplete motions of electrons within the channel that do not result in external current flow do not register as current events in the external circuit. Such motions may involve lots of path retracing within the channel even after a long time interval has passed but will eventually result in a round-trip motion. These motions are all part of the normal randomness that causes variance in event arrival times in a Poisson process. The external voltage source may be viewed as a small-signal short that couples electrons that come in at one end directly to the other end with an almost-zero delay. Thus, the diffusive motions may be viewed as occurring on a loop such that the point of origin of an electron in the channel does not matter. Figure 7.6 (a) and Figure 7.6 (b) illustrate that the mean travel time for an anticlockwise journey and a clockwise journey are the same since $L_1 + L_2 = L_2 + L_1 = L$, respectively. Figure 7.6 (c) and Figure 7.6 (d) illustrate that the mean travel time is also

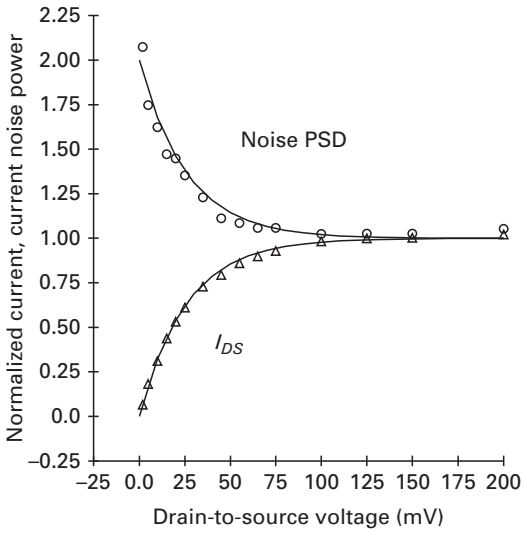

Figure 7.7. Experimentally measured power spectral density of drain-current noise in a subthreshold MOS transistor as the region of operation of the device is varied from linear to saturation. Reprinted with kind permission from [2] (©1993 IEEE).

density in the linear region, $4qI_{DSAT}$. Figure 7.7 shows the first experimental measurements of the electronic current and power spectral density of noise in subthreshold MOS transistors [2]. The measurements are in good accord with Equations (7.24) and (7.23), respectively. The power spectral density of the noise in the subthreshold transistor decreases by a half because the total charge in the device is reduced by a half as we move from the linear region to the saturation region. Alternatively, if we view the external current as being composed of the difference between a forward anticlockwise current of I_F and a reverse clockwise current of I_R, Equations (7.23) and (7.24) are analogous to stating that

$$\begin{aligned} I_{ds} &= I_F - I_R \\ I_F &= I_{DSAT} \\ I_R &= I_F e^{-V_{DS}/\phi_t} \\ \overline{\Delta I_{ds}^2} &= 2q(I_F + I_R)\Delta f. \end{aligned} \tag{7.25}$$

Thus, in this interpretation, the noise spectral density is due to the sum of the shot noise of a forward diffusion current and a reverse diffusion current. It reduces by a factor of two as we move from the linear region to the saturation region because the shot noise of the reverse current, which is equal to that of the forward current when $V_{DS} = 0$, goes to zero as the reverse current goes to zero. Equation (7.25) reveals that the variance of the difference of two currents is maximal when both are present even though the mean is minimal at this point, a straightforward application of Equations (7.15) and (7.16), with $\alpha_1 = 1$ and $\alpha_2 = 1$. Figure 7.8 also reveals that

7.12 Some caveats about noise

Purely reactive devices like inductors, capacitors, masses, springs, i.e., devices that store energy but do not dissipate it as heat, do not exhibit noise. They do not exhibit noise because of a fundamental theorem known as the fluctuation-dissipation theorem [15]. The theorem states that in order for a device to exhibit thermal fluctuations, it must dissipate energy. The physical insight behind the theorem is that dissipation couples a device to the many degrees of freedom of the heat reservoir that always surrounds it. The device dissipates energy into these degrees of freedom and these degrees of freedom, in turn, pour energy back into the device which manifests as noise. If a device is ideal and lossless, then it is not coupled to its surroundings, nothing can affect it, and therefore it does not exhibit noise. The fluctuation-dissipation theorem is a generalization of the Nyquist-Johnson formula for noise in an electrical resistor, i.e., $\overline{\Delta I_{res}^2} = 4kTG\Delta f$, to noise in any device that dissipates energy whether mechanical, chemical, etc. In Chapter 8, we shall use this theorem to compute noise in mechanical MEMS resonators. In Chapter 24, we shall use the concepts of noise discussed in this chapter and in Chapter 8 to compute noise fluxes in chemical reactions.

Small-signal resistances that are not physical but that merely arise from definitions, e.g. r_π and r_o, which are small-signal ac resistances (obtained by linearizing the I–V curve of the transistor about an operating point) do not exhibit noise. On the other hand, real resistances like r_S and r_G that may be present at the source or gate terminals do exhibit noise.

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stiffness forces balance any electrostatic force mismatch. One undesirable consequence of the capacitor mismatch is that a false dc acceleration is reported at the output of the lock-in amplifier (the output after demodulation and filtering) when none exists. Fortunately, in the vibration sensor that we have described such an effect is easily cancelled: the dc value of the lock-in amplifier's output is fed back to alter the dc value of one of the static plates in a negative-feedback loop such that electrostatic forces reestablish exact equality in the capacitances [1]. The closed-loop bandwidth of this negative-feedback loop is set around 1 Hz to create the highpass cutoff frequency of the vibration sensor.

Electrostatic force feedback is frequently used in BioMEMS applications to create oscillations in MEMS resonators. In these cases, positive feedback rather than negative feedback is utilized to excite the oscillation [2]. It is worth noting that the C_0/x_0 dependence of the force in Equation (8.37) results in a negative electrostatic spring stiffness due to positive feedback in any application: the closer two capacitive plates get, the stronger is the electrostatic force between them, which brings the plates even closer together. For overall stability in non-oscillatory applications, the normal positive spring stiffness must exceed the negative spring stiffness set by electrostatics. The MEMS example of this chapter provides useful background for the BioMEMS applications discussed in Chapter 20.

Chapters 7 and 8 conclude our treatment of noise. The material of these chapters is important for a deeper understanding of several chapters in the book, including Chapters 11, 12, 13, 14, 15, 18, 19, 20, 22, and 24. These chapters also provide further examples of low-noise low-power circuits.

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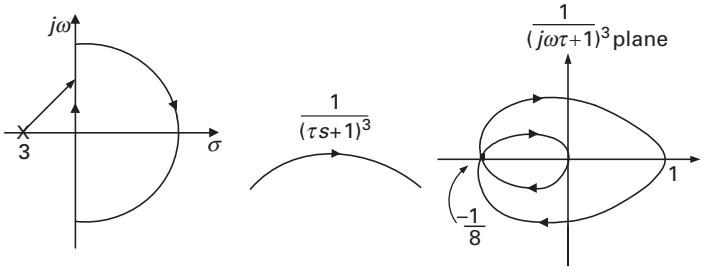

Figure 9.5. Nyquist plot of the phase-shift oscillator example.

the magnitude is 0 and the overall phase is $-270°$. For physical systems, the magnitude of $a(j\omega)f(j\omega)$ is an even function of ω while the phase is an odd function of ω. The Nyquist plot for negative frequencies is then an exact replica of that for positive frequencies except that it is mirrored about the real axis such that $a(-j\omega)f(-j\omega) = [a(j\omega)f(j\omega)]^*$, i.e., complex-conjugate symmetry is preserved.

Figure 9.5 shows that for $0 \leq K \leq 8$, the $-1/K$ point falls outside both encirclements of the Nyquist plot. For $K > 8$, the $-1/K$ point is encircled twice by two clockwise encirclements corresponding to $N = 2$. Since $P = 0$, $Z = N + P = 2$, i.e., we have two zeros of $1 + Ka(s)f(s)$ in the RHP for $K > 8$, indicating instability for these K. The Nyquist diagram is consistent with our root-locus answer. In fact, it provides additional information as well. We note that for $K < -1$, the $-1/K$ point has one encirclement corresponding to one unstable pole for these K. The latter case corresponds to the case of positive feedback since K is negative and corresponds to the finding that the phase-shift oscillator is unstable if the positive-feedback loop gain exceeds 1. Root-locus plots for positive feedback are discussed later in this chapter and yield the same answer. For the phase-shift oscillator, the root-locus plot for positive feedback has three asymptotes making angles of 0°, 120°, and 240° with the real axis; the 0° asymptote leads to the unstable RHP pole for $|K| > 1$, i.e., $K < -1$.

The example of Figure 9.5 reveals that the Nyquist plot and root-locus techniques yield similar information. However, the Nyquist method can use experimental information from Bode plots of $a(j\omega)f(j\omega)$ even if knowledge about the poles and zeros of $a(s)f(s)$ is not available. Nyquist techniques can therefore function when root-locus techniques fail and are consequently more general.

9.2 Nyquist-based criteria for robustness: Gain margin and phase margin

From the following algebraic manipulations on Black's formula

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a(s)}{1 + a(s)f(s)} = \frac{1}{f(s)}\left[\frac{a(s)f(s)}{1 + a(s)f(s)}\right] = \frac{1}{f(s)}\left[\frac{L(s)}{1 + L(s)}\right], \tag{9.3}$$

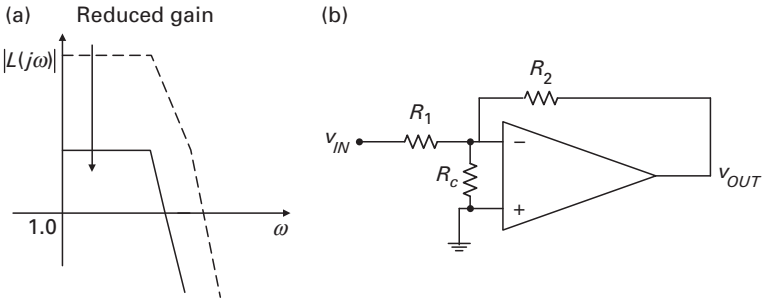

Figure 9.9a, b. Reduced-gain compensation: (a) Bode plot and (b) circuit example.

crossover frequency. There are five common compensation techniques, which we describe below [2].

9.3.1 Reduced-gain compensation

In this scheme, the loop gain of the feedback loop is simply lowered until there is acceptable phase margin. Figure 9.9 (a) reveals an example Bode plot of a loop transmission (a log-log plot of $|L(j\omega)|$ vs. ω) before and after compensation. By simply lowering the loop gain, the unity-gain crossover frequency is forcibly lowered such that phase contributions from only one of the two poles in $|L(j\omega)|$ are significant near crossover. Thus, the phase margin improves from nearly 0° in the uncompensated case where both poles contribute an almost full −90° of phase each, to nearly 90° in the compensated case where only one pole contributes −90°. Figure 9.9 (b) reveals an inverting-amplifier circuit example which uses this form of compensation. The presence of R_c between the v_- and v_+ inputs of the operational amplifier alters the loop gain of the uncompensated system from

$$\frac{A_v(s)G_2}{G_2+G_1} \quad \text{to} \quad \frac{A_v(s)G_2}{G_2+G_1+G_c} \tag{9.9}$$

in the compensated system without noticeably affecting the overall closed-loop gain at low frequencies where $|A_v(s)| \gg 1$. Here, $A_v(s)$ is the operational-amplifier gain, and $G_i = 1/R_i$. While the compensation improves the transient performance of the loop considerably, the loop's crossover frequency and consequently closed-loop bandwidth are considerably reduced. Equation (9.3) reveals that a closed-loop system's frequency response begins to significantly deviate from its ideal $1/f(j\omega)$ behavior near and after $|L(j\omega)| = 1$; thus, the closed-loop bandwidth, i.e., the range of frequencies over which ideal behavior is exhibited, scales with the loop's unity-gain or crossover frequency.

9.3.2 Dominant-pole compensation

In this scheme, a slow large-time-constant system is introduced into the loop such that, near the loop's crossover frequency, the dynamics of the loop transmission

feedback path gain and major loop gain are at their highest values such that a good phase margin for this case guarantees a good phase margin for other cases where the feedback path gain has an attenuating value, and the major loop gain and crossover frequency are consequently lower. The shape of the net transmission is controlled by a well-defined passive component C_c and the minor loop has about 90° of phase margin as well.

9.4 The closed-loop two-pole τ-and-Q rules for feedback systems

Frequently, well-behaved loop transmissions in circuit design can be approximated with a feedback loop that has two time constants and a dc loop gain A_{lp} especially near their crossover frequency:

$$L(s) = A_{lp}\left(\frac{1}{\tau_{big}s + 1}\right)\left(\frac{1}{\tau_{sml}s + 1}\right) \tag{9.12}$$

The closed-loop transfer function of a system with this loop transmission entirely in its feedforward path and with a unity-gain feedback path is then given by

$$\begin{aligned} H_{cl}(s) &= \frac{L(s)}{1 + L(s)} \\ &= \frac{\left(\dfrac{A_{lp}}{A_{lp} + 1}\right)}{\dfrac{\tau_{big}\tau_{sml}}{A_{lp} + 1}s^2 + \dfrac{(\tau_{big} + \tau_{sml})}{A_{lp} + 1}s + 1} \end{aligned} \tag{9.13}$$

Equation (9.13) can be rewritten in a form that describes the closed-loop system as a second-order system with its transfer function in a canonical form

$$H_{cl}(s) = \frac{A_{cl}}{\tau_{cl}^2 s^2 + \dfrac{\tau_{cl}s}{Q_{cl}} + 1} \tag{9.14}$$

By performing some simple algebra on Equation (9.13), the values of A_{cl}, τ_{cl}, and Q_{cl} in Equation (9.14) can be found to be

$$\begin{aligned} A_{cl} &= \frac{A_{lp}}{A_{lp} + 1} \\ \frac{1}{\tau_{cl}} = \omega_n &= \sqrt{\frac{1 + A_{lp}}{\tau_{sml}\tau_{big}}} \\ Q_{cl} &= \frac{\sqrt{(1 + A_{lp})}}{\sqrt{\dfrac{\tau_{big}}{\tau_{sml}}} + \sqrt{\dfrac{\tau_{sml}}{\tau_{big}}}} \end{aligned} \tag{9.15}$$

$$\frac{v_{out}(s)}{i_{in}(s)} = \frac{1}{g_f}\left(\frac{\kappa_s A/(1+\kappa_s A)}{1+\frac{s(C_{in}/g_f)}{1+\kappa_s A}}\right)$$

$$\text{where } g_f = \frac{I_{IN}}{\kappa_s(kT/q)} \tag{11.3}$$

$$\Rightarrow v_{out}(s) = \frac{kT}{\kappa_s q}\left(\frac{i_{in}}{I_{IN}}\right)\left(\frac{\kappa_s A/(1+\kappa_s A)}{1+\frac{s(C_{in}/g_f)}{1+\kappa_s A}}\right)$$

Since i_{in} is a small change in the operating-point current of I_{IN} , i.e., $i_{in} = \Delta I_{IN}$, Equation (11.3) may be re-expressed as

$$v_{out}(s) = \frac{kT}{\kappa_s q}\left(\frac{\Delta I_{IN}(s)}{I_{IN}}\right)\left(\frac{\kappa_s A/(1+A)}{1+\frac{s(C_{in}/g_f)}{1+\kappa_s A}}\right) \tag{11.4}$$

Thus, at any operating point I_{IN}, the logarithmic transimpedance amplifier transduces small fractional changes in its input $\Delta I_{IN}/I_{IN}$ into an output voltage while speeding up the input time constant by $(1 + A)$. Since g_f varies linearly with the input I_{IN} according to Equation (11.3), the small-signal time constant of the logarithmic transimpedance amplifier varies linearly with I_{IN} and is operating-point dependent unlike that of a linear transimpedance amplifier. The logarithmic transimpedance amplifier is capable of wide dynamic range operation with a modest power-supply voltage. Its scale-invariant fractional amplification is beneficial in several applications where percentage changes rather than absolute changes carry information, e.g., objects reflect or absorb a fixed fraction of the light incident on them independent of the light intensity; consequently, it is the relative $\Delta I/I$ contrast in time or space that carries information in a visual image rather than the absolute intensity. The minimum detectable contrast in a logarithmic transimpedance amplifier is input-current-intensity invariant because the bandwidth and consequently integration interval of the system scales with input current such that a constant number of electrons is always gathered during sensing. In a linear transimpedance amplifier, the bandwidth and consequently integration interval of the system are fixed such that the minimum detectable contrast is worsened at low input intensities due to the gathering of few electrons and improved at high input intensities due to the gathering of more electrons. A logarithmic transimpedance amplifier effectively functions like a linear transimpedance amplifier with built-in gain control where R_f is changed with I_{IN} such that $I_{IN}R_f$ is a constant. Operation in the logarithmic versus linear domains is analogous to floating-point versus fixed-point operation in digital number systems. Both domains of operation are useful in various applications, with logarithmic transduction being particularly beneficial in systems that need scale-invariant and wide-dynamic-range operation.

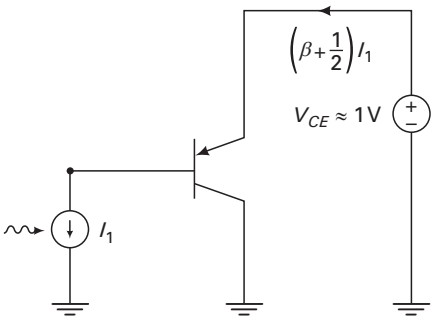

Figure 11.3. A phototransistor. The base terminal is left floating. Incident light generates a photocurrent I_1 at the base that is then multiplied by the transistor's current gain β.

to generate a forward current in the diode that balances its reverse short-circuit current. Thus, if the diode has a characteristic pre-exponential constant of I_S, the open-circuit voltage, v_{OC}, developed by the photodiode is given by

$$v_{OC} = \frac{kT}{q}\ln\left(\frac{i_{PHOTO}}{I_S}\right) \tag{11.7}$$

A phototransistor can be built with a bipolar transistor that has a floating base as shown in an example circuit in Figure 11.3. Each pn junction of the transistor generates a floating photocurrent that attempts to forward bias the collector-to-base junction or the emitter-to-base junction respectively. Since each floating current source can be decomposed into two grounded current sources, the phototransistor may be well approximated by the circuit of Figure 11.3 with a light-dependent base current that is amplified by the β of the bipolar transistor. A phototransistor typically has more input capacitance at its base than does a photodiode generating the same base current. When it is used in a transimpedance-amplifier topology to generate photocurrent, the resulting bandwidth is determined by the slow dynamics at its base rather than by any speedup that may be achieved at its emitter (pnp photocurrent) or at its collector (npn photocurrent). The amplification of the photocurrent by β in the transistor does not improve the signal-to-noise ratio of the photodiode since the dominant source of noise in a bipolar transistor is usually base-current shot-noise, which is amplified by the same factor of β as the signal photocurrent. For the same light-collection area, photodiodes typically occupy a smaller area than phototransistors as well. For all of these reasons, photodiodes are usually preferable to phototransistors in most applications.

Figure 11.4 shows the host of pn junctions available in a normal CMOS process that can be used to create photodiodes or phototransistors. Figure 11.5 shows the host of pn junctions available in a BiCMOS process that can be used to create photodiodes or phototransistors. BiCMOS processes include an additional p-base layer, which increases the number of available photodevices. Not all of these junctions are equally effective in transducing light to electrons. Figure 11.6 (a)

ultra-low-power pulse oximeter, a medical instrument for noninvasive measurement of the oxygen saturation level of hemoglobin in the blood via the use of infrared and red LEDs and photoreceptors [2]. The pulse oximeter is further described in Chapter 20.

Figure 11.8 (a) reveals the circuit of the photoreceptor. The transistor M_3, the light-dependent current I_l, and C_{in} form a source follower, which is shown in Figure 11.8 (b) as a subcircuit. The transistors M_1, M_2, and M_4 form a high-gain amplifier with a load capacitance C_0, which is shown in Figure 11.8 (c) as a subcircuit. The capacitors C_1 and C_2 form a capacitive divider, which is shown in Figure 11.8 (d) as a subcircuit. The element R_A in Figure 11.8 (a) represents a very large adaptation resistance whose conductance is insignificant compared with the admittance of capacitance C_1 at all but the lowest frequencies. We shall approximate it as having an infinite resistance unless otherwise mentioned. We shall discuss how R_A is implemented with two back-to-back diode-like resistances in parallel after discussing the rest of the circuit.

The overall topology of Figure 11.8 (a) is similar to that of the logarithmic transimpedance amplifier of Figure 11.1 (b) with I_l as an input, M_3 as the feedback transistor, and the high-gain amplifier comprised of M_1, M_2, M_4 and C_0. However, the reference voltage V_{REF} is implicitly established by the high-gain amplifier subcircuit. Furthermore, the capacitive-divider and R_A form a frequency-shaping attenuation network in the feedback path that causes the ac gain to be higher than the dc gain at all but the lowest frequencies. At equilibrium, the negative-feedback loop establishes operating-point parameters such that I_l flows through M_3 and the voltage v_{IN} is at an implicit reference value such that the current through M_1 and M_2 is equal to that of the bias current of M_4.

The transistor M_2 in Figure 11.8 (c) functions as a cascode transistor to prevent the C_{gd} capacitance of M_1 from loading the input node V_{in} with a Miller capacitance of value $C_{gd}(1+A)$, where A is the gain of the amplifier. Such loading is detrimental to the bandwidth of the photoreceptor. It also increases the output impedance and the gain of the amplifier through the usual mechanism of a cascoding transistor (Equation (10.36) in Chapter 10). We can show that the small-signal equivalent circuit of the high-gain amplifier of Figure 11.8 (c) is that of Figure 11.9 with an output impedance r_o, gain A, and input-referred noise power per unit bandwidth $v_n^2(f)$ given by

$$\begin{aligned} r_0 &= r_0^{M_4} // (r_0^{M_2}(1+g_s r_0^{M_1}) + r_0^{M_1}) \approx r_0^{M_4} \\ g_A &= \kappa g_s = \frac{\kappa I_A}{\phi_t} = g_m \text{ of } M_1 \\ A &= \frac{v_{out}}{v_{in}} = -g_A r_0 \\ v_n^2(f) &= \frac{4qI_A}{g_A^2} \end{aligned} \tag{11.9}$$

We have assumed that all transistors operate in saturation. Only the $2qI_A$ shot-noise contributions of subthreshold transistors M_1 and M_4 affect the noise of the

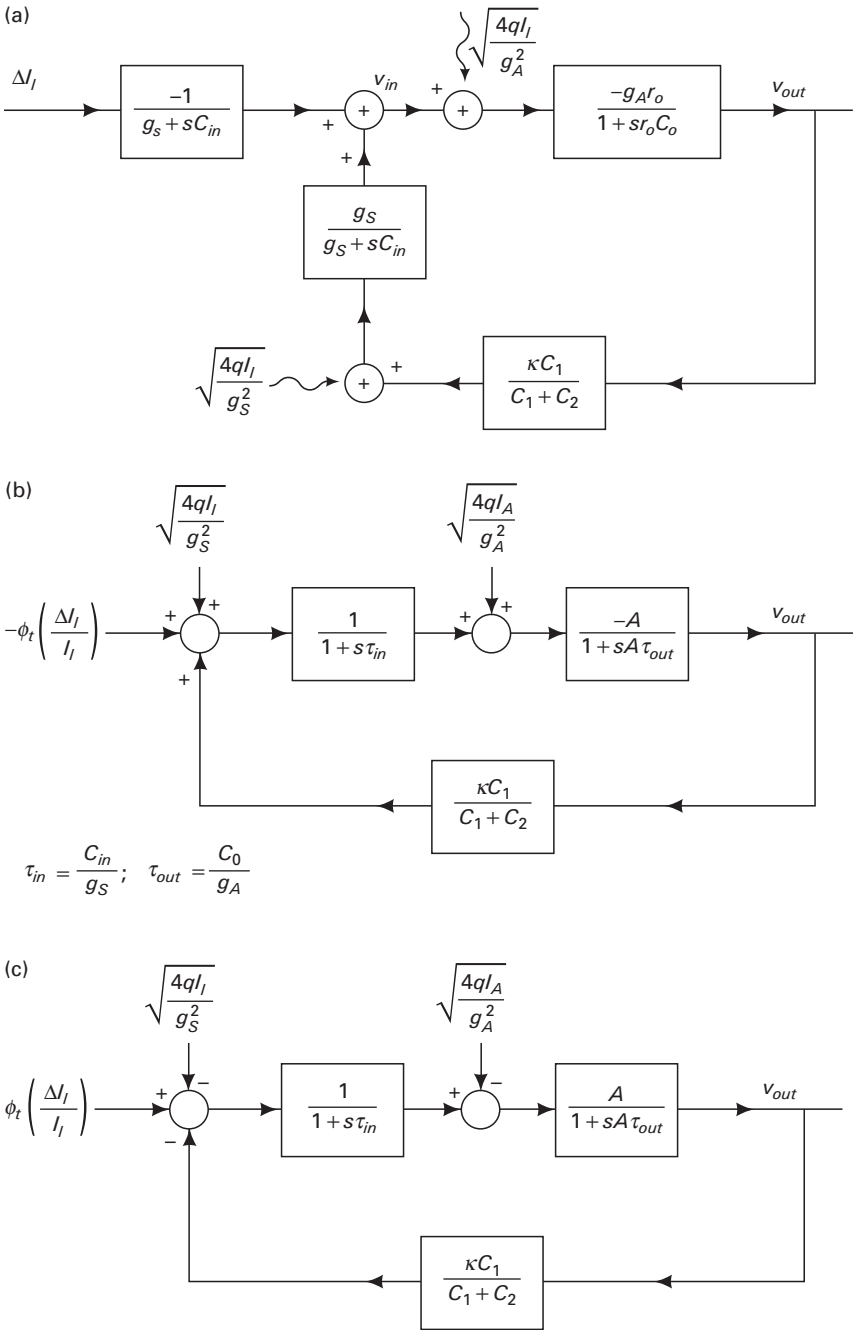

Figure 11.10a, b, c. Feedback block diagrams of the adaptive photoreceptor: (a) original form, (b) and (c) two simplified forms.

contribution of its noise to the output is usually small. Since g_A needs to be almost A^2/A_{cl} greater than g_s for good phase margin, the noise per unit bandwidth of the amplifier is almost A_{cl}/A^2 times smaller than that due to the source follower. The increase of the amplifier's noise by the zero increases its contribution by a factor of $A_{lp}^2 = (A/A_{cl})^2$ at most, such that the amplifier's noise per unit bandwidth over all frequencies within the closed-loop bandwidth is still only $1/A_{cl}$ times that of the source-follower's noise per unit bandwidth at most. *Thus, in most practical situations, the noise of the photoreceptor is dominated by the source-follower noise and the amplifier's noise may be neglected.*

From the analysis of the source-follower's noise in Chapter 8, we can compute that the minimum detectable contrast for a simple source-follower photoreceptor with no transimpedance-amplifier speedup is given by

$$\begin{aligned} \frac{\Delta I_l^2}{g_s^2} &= \frac{kT}{C_{in}} \\ \text{i.e. } \frac{\Delta I_l^2}{I_l^2} &= \frac{kT}{C_{in}} \times \frac{1}{\phi_t^2} = \frac{q}{C_{in}\phi_t} \end{aligned} \tag{11.22}$$

With a speedup of $(1 + A_{lp})$, the closed-loop bandwidth is increased such that the total noise is increased. Thus, the minimum detectable contrast is increased and is given by Equation (11.23) below:

$$\begin{aligned} \frac{\Delta I_l^2}{I_l^2} &= \frac{q}{C_{in}\phi_t}(1 + A_{lp}) \\ \text{i.e. } \left(\frac{\Delta I_l}{I_l}\right) &= \sqrt{\frac{q}{C_{in}\phi_t}(1 + A_{lp})} \end{aligned} \tag{11.23}$$

Figure 11.13 and the associated caption, which are adapted from [1], present measurements of the output noise of the photoreceptor of Figure 11.8 and the source follower of Figure 11.7. The photoreceptor simply amplifies the noise per unit bandwidth of the source-follower by about as much as it amplifies an intentional periodic LED light input (the tone inputs in Figure 11.13). Thus, it is hardly increasing the input-referred noise per unit bandwidth but it does increase the bandwidth of the system, and therefore the total input-referred noise and minimum detectable contrast. The bandwidth of the noise is the largest when the cascode transistor M_2 is used.

Equation (11.23) suggests that a good photoreceptor with a small minimum detectable contrast must have a large capacitance. Such a photoreceptor can be built by scaling up the area of the photodiode until the intrinsic bandwidth of the photodiode self limits (since I_l, g_s, and the depletion capacitance C_{dep} of the photodiode all scale with its area); A_{lp} is chosen to yield the desired speedup needed at the lowest light intensities and I_A is chosen to yield stability at the highest light intensities; then, from Equation (11.23), the size of the photodiode needed to yield the minimum detectable contrast can be computed. A 100 pF value of C_{in} and $A_{lp} = 35$ yields a minimum detectable contrast of nearly 0.16%.

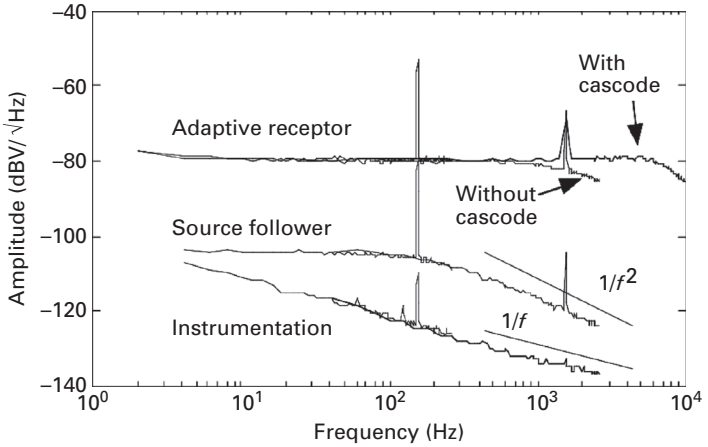

Figure 11.13. Experimentally measured output noise spectra of the adaptive photoreceptor and the simple source-follower photoreceptor. The input-referred noise of the two receptors is almost identical. The noise spectrum of the instrumentation used for making the measurement is also shown for convenience. Reprinted with kind permission from [1] (©1994 IEEE).

11.6 The adaptation resistor R_A

Figure 11.14 shows how the adaptation resistor R_A, thus far assumed to be infinite, is constructed with two back-to-back diode-like elements [1]. The device is made with a single well transistor such that an MOS transistor is operative when $V_{out} = V_0 > V_f$ in Figures 11.8 (a) and 11.14, respectively, and the parasitic bipolar transistors present in every MOS transistor are operative when $V_0 < V_f$. The lateral bipolar transistor revealed in Figure 11.14 typically plays a much smaller part than the vertical bipolar transistor due to the vertical bipolar's significantly better β. Thus the circuit model shown in Figure 11.15 (a) only analyzes the functioning of R_A with one vertical bipolar transistor. It also explicitly adds parasitic photocurrents that appear in any real photoreceptor due to unwanted light leakage onto the pn junctions of R_A. The large ${I_{well}}^p$ parasitic photocurrent due to the well-substrate junction is absorbed into the bias current of M_4 in Figure 11.8 and does not affect the circuit's operation much, one of the benefits of this configuration. Any stray electrons that diffuse into the n-well region are also absorbed. Figure 11.15 (b) reveals the exponential I–V curves (with slopes differing by a factor of κ) that result from the subthreshold MOS transistor and the bipolar transistor.

Simple analysis of the circuit of Figure 11.15 (a) yields:

$$\begin{aligned} i &= i_M - i_B + I_{par} \\ \Delta V &= v_{OUT} - v_F \\ i_M &= I_0 e^{\kappa \Delta V/\phi_t}\left(1 - e^{-\Delta V/\phi_t}\right) \\ i_B &= \frac{I_s}{\beta}\left(e^{-\Delta V/\phi_t} - 1\right) \text{ at } v_{OUT} \text{ side} \\ &= I_s\left(e^{-\Delta V/\phi_t} - 1\right) \text{ at } v_F \text{ side} \end{aligned} \tag{11.24}$$

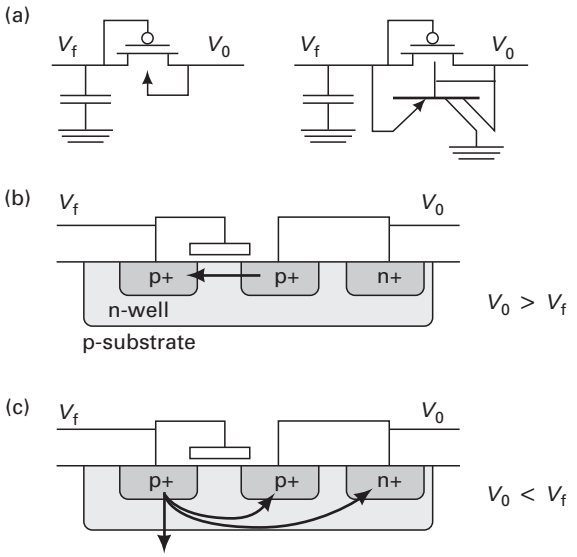

Figure 11.14a, b, c. The adaptive element used in the photoreceptor: (a) shown in two schematic forms, (b) conducting as an MOS transistor and (c) conducting as a bipolar transistor with two collectors. Reprinted with kind permission from [1] (©1994 IEEE).

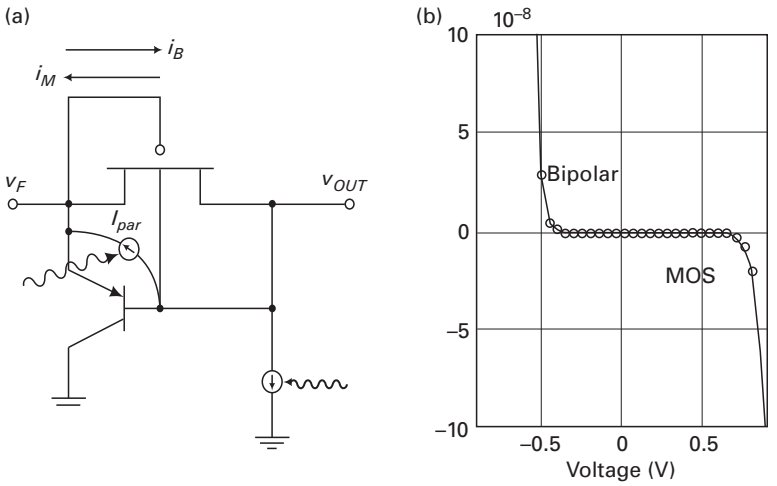

Figure 11.15a, b. The adaptive element: (a) transistor-level schematic including parasitic photocurrents and (b) experimentally measured $I - V$ curves, showing that the element behaves like two back-to-back diodes. Reprinted with kind permission from [1] (©1994 IEEE).

From Figures 11.15 (a) and 11.8 (a), we can conclude that the gate-node (the v_F node) conductance at equilibrium $G_A = 1/R_A$ determines the value of a zero located at $-1/R_A C_1$ beyond which the attenuation of the $R_A - C_1 - C_2$ frequency-shaping lead network begins and the location of a pole at $1/R_A(C_1 \| C_2)$ at which it asymptotes. The value of G_A can be determined from small-signal

In Figure 12.6 (b), the bump transistors have been ratioed to have a W/L that is w times larger than those of their diode-connected input transistors. The derivation below then reveals that

$$i_{OUT} = i_+ - i_-; i_B = i_+ + i_- + w\frac{i_+ i_-}{i_+ + i_-}; i_+ = e^{\frac{\kappa v_+}{\phi_t}}; i_- = e^{\frac{\kappa v_-}{\phi_t}}$$
$$\boxed{i_{OUT} = i_B \frac{\sinh x}{\beta + \cosh x} \text{ where } \beta = 1 + \frac{w}{2} \text{ and } x = \frac{\kappa(v_+ - v_-)}{\phi_t}} \tag{12.10}$$

If $w = 2$ such that $\beta = 2$ as well, then i_{OUT} is maximally linear in that its Taylor series expansion with x has no third-order term:

$$\frac{\sinh x}{2 + \cosh x} = \frac{x}{3} - \frac{x^5}{540} + \frac{x^7}{4536} - \frac{x^9}{77760} + \cdots \tag{12.11}$$

In comparison, a conventional differential pair without the bump transistors would have an output current described by

$$\tanh\frac{x}{2} = \frac{x}{2} - \frac{x^3}{24} + \frac{x^5}{240} - \frac{17x^7}{40320} + \cdots \tag{12.12}$$

By comparing the coefficients of the linear term in Equations (12.11) and (12.12), we find that a bump-linearized differential pair with $w = 2$ has lower transconductance by a factor of $3/2$ at the origin and is also significantly more linear than a tanh function. The lowered factor for transconductance is intuitive since at $w = 2$, the bump arm and each of the two differential arms each have a current of $I_B/3$ rather than $I_B/2$ in a differential pair.

If w is extremely large, the transconductance at the origin reduces considerably (by a factor of $4/(4 + w)$) but the saturation current is unchanged such that the I–V curve of the circuit of Figure 12.6 (b) exhibits a flat expansive dead zone at the origin followed by a compressive return to output saturation. If w is small, the transconductance is attenuated throughout without any changes from expansivity to compressivity. At $w = 2$, the expansive nature of the curve at the origin is exactly compensated for by the compressive nature of saturation such that maximally linear operation is achieved.

The net result of bump linearization at $w = 2$ is that the effective linear range is increased by $3/2$. This linear range increase is also seen in the WLR circuit of Figure 12.2, such that the overall linear range is given by modifying Equation (12.5) by a factor of $3/2$:

$$V_L = \frac{3}{2} \times \frac{2\phi_t}{1 - \kappa}\left(1 + \frac{1}{\kappa_p} + \frac{\kappa}{\kappa_n}\right) = \frac{3\phi_t}{1 - \kappa}\left(1 + \frac{1}{\kappa_p} + \frac{\kappa}{\kappa_n}\right) \tag{12.13}$$

Figure 12.7 (a) reveals experimental data for a WLR circuit for various different values of w. We see that, at $w = 0$, the I–V curve of the WLR is well fit by a tanh curve with $V_L = 1.16$ V. Even large w's only cause gentle distortion suggesting that achieving $w = 2$ exactly is not critical and consequently that the WLR circuit is well tolerant of mismatch in w. Figure 12.7 (b) reveals that the $3/2$ increase in

its gain with sophisticated automatic-gain-control circuitry such that we do not have to manually turn a knob to sense soft signals versus loud signals as we do in an oscilloscope.

We find experimentally that the white-noise term dominates over the $1/f$ noise term in determining the output *SNR* of our filter because the use of large mostly pFET transistors reduces the value of K_f, because white noise is often dominant in ultra-low-power subthreshold circuits, and because frequencies below 1 Hz are filtered out by offset-adaptation circuits. Thus, if we only keep the white-noise term in Equation (12.24), we find that

$$SNR = \frac{2CV_L}{Nq} \tag{12.25}$$

Thus, *if white noise dominates our system*, *more linear range implies more dynamic range*. If the bias current of the amplifier is I_B, the bandwidth of the filter f_c is given by

$$f_c = \frac{I_B}{2\pi CV_L} \tag{12.26}$$

We can then compute the power needed to attain a given bandwidth and *SNR* to be

$$\begin{aligned} P &= 2V_{DD}I_B \\ P &= 2V_{DD}(2\pi f_c CV_L) \\ \boxed{P &= (V_{DD}\pi Nq)(f_c)(SNR)} \end{aligned} \tag{12.27}$$

Thus, *we see that it costs power to attain precision* (SNR) *and bandwidth*, *a lesson true in all circuits*. The cost of getting a better signal-to-noise ratio with a wider linear range amplifier V_L is not free. The wider linear range improves signal-to-noise ratio because the maximal signal power scales like V_L^2 while the noise power scales like V_L such that there is a net improvement in *SNR* that scales like V_L. But the reason that the noise power only scales like V_L even though the input-referred noise per unit bandwidth scales like V_L^2 is that the bandwidth f_c which scales like I_B/V_L is reduced thus leading to more averaging. Thus, if I_B is kept constant between two designs, one of which has a large V_L and the other of which has a small V_L, the large-V_L design will have large *SNR* and a small bandwidth while the small-V_L design will have small *SNR* and large bandwidth. Thus, to maintain bandwidth at the value possessed by a small-V_L design, we need to increase I_B proportionately with V_L in a large-V_L design. The bandwidth increase achieved by increasing I_B does not increase the noise and maintains the *SNR* at that given by Equation (12.25). Though there is less averaging in the latter case, the input-referred noise per unit bandwidth falls such that the total output noise is only determined by the capacitance and topology and independent of I_B as we've seen on multiple occasions.

Figure 12.18 (a) illustrates that, in a thermal-noise-limited design, if V_L is increased, the noise per unit bandwidth increases proportionately with V_L^2 and

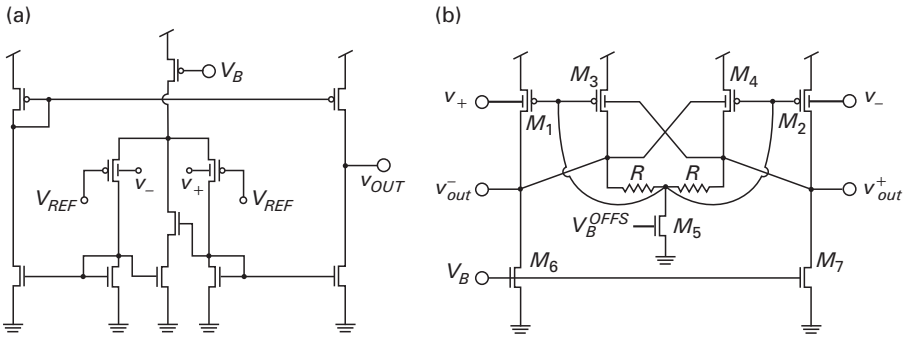

Figure 12.19a, b. A low-voltage subthreshold transconductance amplifier is shown in (a) and a low-voltage above-threshold transconductance amplifier is shown in (b). Reproduced with kind permission from [4] (©2005 IEEE).

processes, a linear range that exceeds V_{DD} is not needed: a linear range of $V_{DD}/2$ provides rail-to-rail operation with a common mode voltage of $V_{DD}/2$. Such a linear range can be obtained by using a subset of the linearization techniques described in this chapter rather than by using all of them. Figure 12.19 (a) reveals a subthreshold design suited for low-voltage operation and Figure 12.19 (b) reveals an above-threshold design suited for low-voltage operation [4]. Before we describe either design, we shall briefly digress to discuss seven general principles for low-voltage analog design. We shall then show how these principles manifest themselves in the particular circuits of Figure 12.19 (a) and 12.19 (b).

1. Since each transistor in a series stack causes a loss in saturated operating range of at least V_{DSAT} (V_{GS} if the transistor is diode connected), *series stacking of transistors should be minimized* in low-voltage designs.
2. *Weak-inversion operation* minimizes V_{DSAT}; therefore, unless high-speed requirements do not prohibit its use, it is preferable in low-voltage operation.
3. It is advantageous to not set the well-to-source voltage $v_{WS} = 0$ but to *use* v_{WS} *as a degree of freedom in low-voltage design*: the well can serve to modulate the dc biasing current while the gate serves as the primary ac input, or vice versa. The use of two control inputs rather than one is always advantageous as we have seen in the example of gate degeneration but it is particularly so in low-voltage design. If only one control input is used, say v_{GS}, the dc voltage V_{GS} must equal $V_{DD}/2$ to maximize voltage headroom; deviations in V_{GS} from $V_{DD}/2$, which are needed to alter the dc biasing current, will then compromise voltage headroom on the v_{gs} ac input at either the top or the bottom rail; however, if V_{WS} is also available as a control input, V_{GS} can be fixed at $V_{DD}/2$ maximizing input ac voltage headroom while V_{WS} can be varied to alter the dc biasing current.
4. If V_{DD} is small and less than the junction turn-on voltage, V_{WS} *can be biased* to be $-V_{DD}$ without danger of turning on the parasitic bipolar transistor in Figure 12.8. Thus, V_{T0} can be reduced to improve overdrive gate voltage in strong inversion, and rail-to-rail operation on the well voltage may be possible.

Table 13.2 Parameters of a resonant lowpass transfer function in various representations

	a and b	ω_n and Q	ω_n and Θ	ω_n and θ
Underdamped region	$a > 0, b > 0$	$0.5 < Q < \infty$	$0 < \Theta < \pi/2$	$0 < \theta < \pi$
Gain > 1 region	$0 < a < b$	$1/\sqrt{2} < Q < \infty$	$0 < \Theta < \pi/4$	$0 < \theta < \pi/2$
Damping	$a/\sqrt{a^2 + b^2}$	$1/(2Q)$	$\sin\Theta$	$\sin(\theta/2)$
Peak frequency	$\sqrt{b^2 - a^2}$	$\omega_n\sqrt{1 - 1/(2Q^2)}$	$\omega_n\sqrt{\cos 2\Theta}$	$\omega_n\sqrt{\cos\theta}$
Peak gain	$(a^2 + b^2)/2ab$	$Q/\left(\sqrt{1 - 1/(4Q^2)}\right)$	$1/(\sin 2\Theta)$	$1/(\sin\theta)$
$-90°$ frequency	$\sqrt{a^2 + b^2}$	ω_n	ω_n	ω_n
$-90°$ frequency gain	$\sqrt{1 + b^2/a^2/2}$	Q	$1/(2\sin\Theta)$	$\dfrac{1}{2\sin(\theta/2)}$
Unity gain frequency	$\sqrt{2(b^2 - a^2)}$	$\omega_n\sqrt{2 - 1/(Q^2)}$	$\omega_n\sqrt{2\cos 2\Theta}$	$\omega_n\sqrt{2\cos\theta}$
3 dB frequencies	$\dfrac{b^2 - a^2 \pm 2ab}{\sqrt{a^2 + b^2}}$	$\omega_n\left(1 - \dfrac{1}{2Q^2} \pm \dfrac{1}{Q}\sqrt{1 - \dfrac{1}{4Q^2}}\right)$	$\omega_n(\cos 2\Theta \pm \sin 2\Theta)$	$\omega_n(\cos\theta \pm \sin\theta)$

computer than to any practical engineering or physical system. Nevertheless, Table 13.2 parameterizes the properties of resonant lowpass transfer functions in various representations. The ω_n and θ representation is the $-s^2$-plane representation while the ω_n and Θ representation is the usual s-plane representation with $\sin(\Theta) = 1/(2Q)$. Thus, $\theta = 2\Theta$. All of these properties were first derived in the $-s^2$-plane representation and then mapped back to the other representations.

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[2] R. Sarpeshkar, R. F. Lyon and C. A. Mead. A low-power wide-dynamic-range analog VLSI cochlea. *Analog Integrated Circuits and Signal Processing*, **16** (1998), 245–274.

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17.3 The impedance of free space

In Figure 17.1, if the medium is free space, $R = \infty$ everywhere except at very high fields. Thus, just as an infinite one-dimensional transmission line is capable of propagating waves in two directions, the three-dimensional LC mesh of Figure 17.1 is capable of propagating waves in all directions with a speed of propagation given by $c = 1/\sqrt{(\mu\varepsilon)}$, the speed of light, and has a characteristic impedance at any point given by $\eta = \sqrt{(\mu/\varepsilon)}$. The parameter η is referred to as the impedance of free space, which evaluates to $120\pi\,\Omega$. By analogy to the one-dimensional transmission-line case, we also find that $E(x, y, z) = \eta H(x, y, z)$ for a plane wave propagating in any direction.

The impedance of free space η is a constant that scales the impedance of several electromagnetic structures. For example, a co-axial BNC cable with a cylindrical inner conductor of radius r_1, a cylindrical concentric outer conductor of radius r_2, and an insulating material between the conductors characterized by ε and μ has a capacitance C per unit length, inductance L per unit length, and characteristic impedance Z_0 given by

$$\begin{aligned} C &= \frac{2\pi\varepsilon}{\ln\left(\frac{r_2}{r_1}\right)} \\ L &= \frac{\mu}{2\pi}\ln\left(\frac{r_2}{r_1}\right) \\ Z_0 &= \sqrt{\frac{L}{C}} = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\left(\frac{r_2}{r_1}\right) \\ &= \frac{\eta}{2\pi}\ln\left(\frac{r_2}{r_1}\right) \end{aligned} \tag{17.12}$$

17.4 Thevenin-equivalent circuit models of antennas

Accelerating charges or changing currents in a transmitting antenna radiate electromagnetic waves into free space represented by propagating $\boldsymbol{E}$ and $\boldsymbol{H}$ 'far fields' in free space. These radiated far fields, after a time delay determined by the speed of light, cause charges and currents in a receiving antenna to change such that we can say that an energy exchange has occurred between the transmitting antenna and the receiving antenna. The loss of energy in the transmitting antenna causes it to have 'damping' or an effective 'radiation resistance'. The gain in energy in the receiving antenna causes it to develop a source voltage or source current across its terminals that is proportional to the local field strength.

In addition to radiating or receiving electromagnetic energy, antennas also store inductive and capacitive energy in the $\boldsymbol{E}$ and $\boldsymbol{H}$ fields that are present near them, i.e., in their 'near fields'. Such fields are not radiated but effectively function like field lines that begin and end on antenna structures (capacitive E fields) or form

$$V_{DD} \geq 6\left(\frac{\kappa_n \sigma_{vthN} + \kappa_p \sigma_{vthP}}{\kappa_n + \kappa_p}\right) + \phi_t \ln(10) \tag{21.8}$$

From Chapter 6, in a 0.1 μm process, the A_{vth} parameter, which describes the threshold-voltage variation is $\sim$3.2 mV.μm such that a minimum-size $\sim$0.1 μm device has σ_{vthN} and σ_{vthP} at $\sim$32 mV. Equation (21.8) then predicts that $V_{DD} \geq 250$ mV. A symmetric analysis can be performed for the other case where we have a weak PMOS transistor and a strong NMOS transistor, which also yields Equation (21.8). Thus, robustness to transistor mismatch sets a minimum value of V_{DD} that is far in excess of that predicted by gain (50 mV) and noise-margin (100 mV) considerations alone. Of course, the use of non-minimum-size devices will lower σ_{vthN} and σ_{vthP} such that V_{DD} can be lowered at the cost of some increase in switching-capacitance-based and static power consumption (see discussion in next section). As we discuss in Chapter 22, in both the analog and digital domains, robustness and efficiency always trade off with each other.

For most practical power-supply voltages in excess of 100 mV, the gain of a subthreshold CMOS inverter is set by short-channel DIBL effects rather than by saturation effects (see Chapter 6 for a description of DIBL in short-channel transistors). If the DIBL coefficient is given by η, then, from a small-signal analysis similar to that in Equation (21.4), we can compute the inverter gain to be

$$A_{inv} = \frac{\kappa_n + \kappa_p}{\eta_n + \eta_p} \tag{21.9}$$

since, typically, $\kappa > 0.6$ and $\eta < 0.1$, A_{inv} is at least 6.

If V_{DD} is sufficiently large (greater than 100 mV), and we apply a step input to the CMOS inverter, to an excellent approximation, we may assume that only the NMOS transistor is on for a positive step input and that only the PMOS transistor is on for a negative step input. Thus, if we assume that $\kappa_n = \kappa_p = \kappa$ for simplicity, the delay of the CMOS inverter to a step input, T_{inv}, can be computed by calculating the time taken by the on current of either the NMOS or PMOS transistor to discharge or charge its load capacitance C_L by a voltage differential of magnitude V_{DD} respectively:

$$\begin{aligned}
I_{OFF} &= \left(\mu_n C_{ox} \frac{W_n}{L_n} \frac{1-\kappa}{\kappa} \phi_t^2\right) e^{-\kappa V_{Tn}/\phi_t} = \left(\mu_p C_{ox} \frac{W_p}{L_p} \frac{1-\kappa}{\kappa} \phi_t^2\right) e^{-\kappa |V_{Tp}|/\phi_t} \\
I_{OFF} &\approx I_{T0} e^{-\kappa V_{T0}/\phi_t} \\
T_{inv} &= \frac{C_L V_{DD}}{I_{ON}} \\
I_{ON} &= I_{OFF} e^{\kappa V_{DD}/\phi_t} \\
T_{inv} &= \frac{C_L V_{DD}}{I_{OFF}} e^{-\kappa V_{DD}/\phi_t} \\
\boxed{T_{inv} &= \frac{C_L V_{DD}}{I_{T0}} e^{-\kappa (V_{DD} - V_{T0})/\phi_t}}
\end{aligned} \tag{21.10}$$

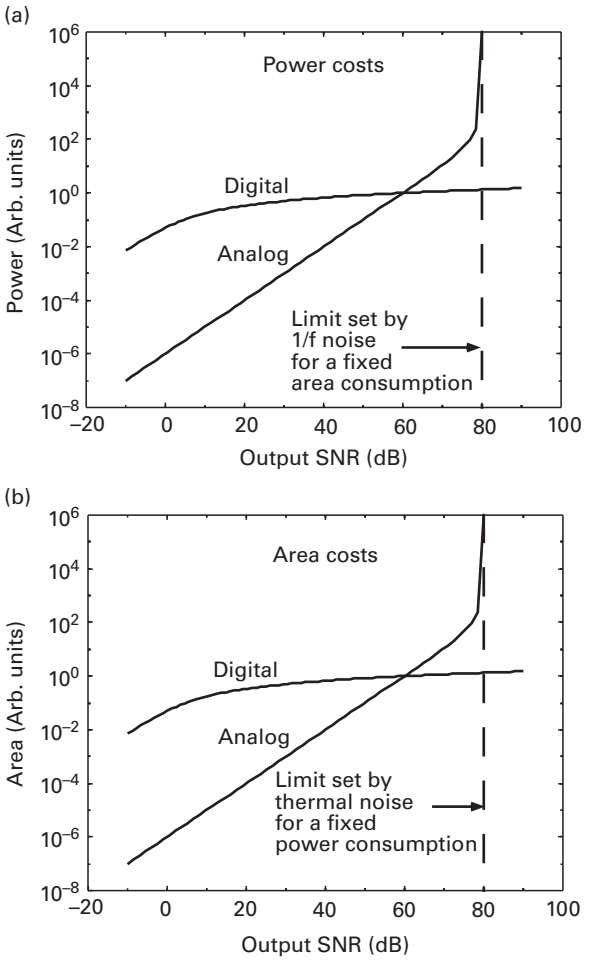

Figure 22.3a, b. Analog-digital crossover curves. Reprinted with kind permission from [11].

Thus, for several computations and typical parameter values corresponding to these computations, a plot of Equations (22.10) and (22.11) in Figures 22.3 (a) and 22.3 (b) reveals that the power and area costs of analog computation are significantly below those of digital computation at low and moderate values of *SNR* respectively.

At large values of *SNR*, maintaining such high *SNR* on a single analog wire requires very low levels of thermal noise and $1/f$ noise, which drastically increases power and area costs for analog computation. In contrast, in digital computation, several 1-bit precise simple logic units can collectively interact with each other to efficiently implement the computation. For example, in the computation of addition, the simple mechanism of a 1-bit carry between adjacent digital adder stages serves to define the overall collective interaction. Thus, the costs for power and area only scale polynomially in the number of bits or logarithmically in the *SNR* as Equation (22.11) reveals. Therefore, Figure 22.3 reveals that at high *SNR* it is

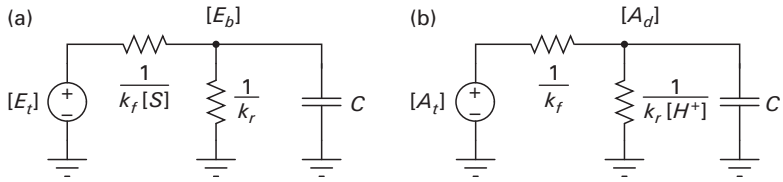

Figure 24.2a, b. Michaelis-Menten association reaction and acid dissociation reaction.

understand Michaelis-Menten kinetics of enzyme-substrate saturation or of another association reaction as resistive-divider saturation.

In many biological systems, typically $[E_b]$ leads to significantly slower production of a product P at a flux rate of $v[E_b]$ via a further unidirectional reaction, accompanied by unbinding of the enzyme and substrate. This reaction is easily represented by including a resistance of value $1/v$ in parallel with the resistance $1/k_r$ in Figure 24.2 (a); in addition, a voltage-dependent transconductance whose output current depends on $[E_b]$ as $v[E_b]$ charges a capacitance $C_2 = 1$; the capacitor's voltage then represents the concentration of P. Thus, simple circuit blocks can also represent Michaelis-Menten kinetics more exactly if needed. However, the essential dynamics of Michaelis-Menten kinetics are well represented by Equations (24.2), (24.3), and Figure 24.2 (a).

A dissociation reaction, e.g., that due to an acid, is given by

$$HA \underset{k_r}{\overset{k_f}{\rightleftharpoons}} H^+ + A^- \tag{24.4}$$

The reader should be able to show that the circuit of Figure 24.2 (b) represents this reaction with $[A_t]$ being the amount of acid in total form (undissociated as $[HA]$ or dissociated as $[A^-] = [A_d]$, i.e., $[A_t] = [HA] + [A_d]$).

Every chemical reaction, e.g., the enzyme-substrate binding illustrated in Figure 24.3, implicitly has two negative-feedback loops embedded within it. The first feedback loop arises because the concentration of reactants falls if the concentration of products builds, thus slowing the forward reaction; this constitutes the major loop of Figure 24.3. The second feedback loop arises because the backward reaction speeds up when the concentration of products builds; this constitutes the minor loop in Figure 24.3. At steady state, the $1/s$ integrator has infinite gain such that the feedback path of the minor loop determines the closed-loop transfer function of the minor loop. Thus, the feedback loop of Figure 24.3 also leads to Michaelis-Menten saturation except that the saturation is now viewed as a high-loop-gain effect with loop gain $[S]/K_d$. The major loop in Figure 24.3 corresponds to the restorative current through resistance $1/k_f$ in Figure 24.2 (a). The minor loop in Figure 24.3 corresponds to the restorative current through $1/k_r$ in Figure 24.2 (a).

One difference between the chemical resistive-divider circuit of Figure 24.2 (a) and actual electronic resistive-divider circuits lies in their noise properties. The current in real resistors flows by drift while their $4kTR$ current noise per unit

24.5 Stochastics in DNA-protein circuits

Poisson noise in mRNA-production flux can be mimicked by Poisson electronic current noise in a manner analogous to that discussed previously for protein-production flux. However, the noise levels in mRNA production for some genes can be high enough such that extremely low currents and extremely small capacitances become necessary in electronics to mimic the same low signal-to-noise ratio (SNR) in biology. The resultant noise in electronics is then not well controlled or predictable. Therefore, it is sometimes advantageous to artificially introduce a controlled level of noise in a relatively quiet electronic circuit to mimic high-noise signals in biology. Figure 24.12 illustrates a circuit for doing so.

In Figure 24.12, the current-mode integrator with output capacitor C and $2I_{R\alpha}$ implement a current-mode version of the $R^{mRNA}C$ lowpass filter in Figure 24.11. That is, $2I_{R\alpha}$ and C correspond to I_A and C in Figure 14.9 in Chapter 14 on current-mode circuits. Similarly, v_{mRNA} and i_{mRNA} correspond to v_{OUT} and i_{OUT} in Figure 14.9 respectively. Instead of a constant $2I_{R\alpha}$ in a traditional current-mode lowpass filter, however, the leak current $2I_{R\alpha}$ is pseudo-randomly switched on and off with a duty cycle of 0.5. Thus, the average value of the leak current that sets the lowpass filter time constant is $I_{R\alpha}$ as in a traditional circuit but the random switching introduces a stochasticity in this leak current. The log voltage on the current-mode capacitor is exponentiated and converted to a current i_{mRNA} that encodes the level of mRNA as in any current-mode circuit. The current i_{mRNA} is gained up by β_{SNR} and used to control the frequency, f_{CCO}, of a current-controlled oscillator (CCO). The output switching frequency of the oscillator is proportional to i_{mRNA} according to $f_{CCO} = \beta_{SNR} i_{mRNA}/q_{CCO}$, where q_{CCO} depends on design parameters internal to the CCO. Thus, as mRNA levels rise, the control current and switching frequency of the CCO rise in proportion. The linear feedback shift register (LFSR) converts the digital output of the CCO to a random switching signal via a classic pseudo-random-number generator technique [13]. Thus, the output of the LFSR randomly switches the $I_{R\alpha}$ current on and off with a switching frequency f_{CCO} that is proportional to the mRNA level encoded by i_{mRNA}. Consequently, as mRNA levels rise, a consequence of a higher mRNA production rate, the arrival

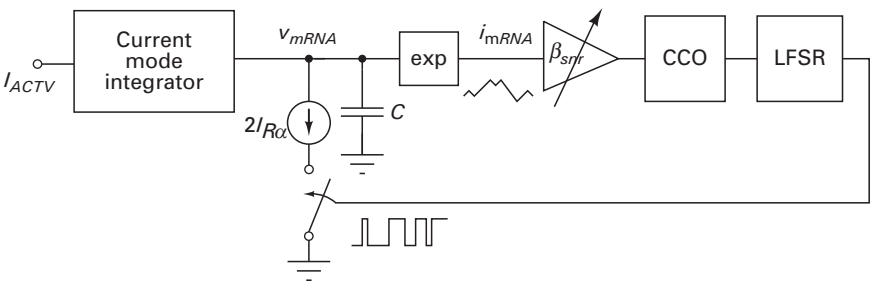

Figure 24.12. Artificial noise generation circuit for low SNR. Reprinted with permission from [14] (©2009 IEEE).

AraC are not simultaneously present; thus, AraBAD protein production is never triggered if glucose is only briefly absent. Figure 24.15 (b) shows that long absences of glucose inducer allow enough time for AraC protein production to build up and reach equilibrium such that sufficiently large amounts of active CRP and AraC are simultaneously present; thus, AraBAD protein production is triggered if glucose is absent for a consistently long duration. Hence, the FFL circuit of Figure 24.14 ensures that the relatively expensive production of proteins needed to process arabinose, a sugar that has a higher cost/benefit ratio than glucose, is only initiated if glucose has been absent for a sufficiently long time.

In many molecular circuits in bacteria and yeast, delays in transcription and translation are relatively negligible compared to mRNA or protein degradation time constants, respectively. Thus, they can often be approximated by increasing these time constants a little. In mammalian cells, however, the delay in the transcription of relatively long genes, which is $\sim$30 minutes, can exceed the mRNA degradation time, which can range from 10 minutes to 10 hours. In certain feedback circuits, the representation of these delays is crucial. Such delays can be programmably represented by conventional clock-counting or one-shot techniques that activate β_{logic} in Figure 24.11 only after a delay. Such delays can be programmably incorporated into the chip from which the data of Figures 24.13 and 24.15 were gathered as described in [14].

24.7 Circuits-and-feedback techniques for systems and synthetic biology

Circuits can often shed insight into biology that is harder to obtain in a different language. For example, work described in [15] has shown how slow outer hair cells in the ear with a time constant of 1 ms can amplify sounds at frequencies over 100 kHz, a two-decade-old mystery. This work shows that while the open-loop time constant of the piezoelectric outer hair cell is 1 ms, the presence of negative feedback in the cochlea with a gain-bandwidth product that is large enough results in a closed-loop system capable of amplification at higher frequencies: the process is analogous to how an operational amplifier with an open-loop time constant of 10 Hz can exploit negative feedback to build an amplifier with a gain of 10^3 at 10 kHz because its gain-bandwidth product is 10^7. In the cochlea, the situation is slightly more complex since the overall negative-feedback loop in the cochlea has a resonance as well, but a simple negative-feedback and root-locus analysis shows that the resonant gain is also improved by negative feedback, thus further enabling high-frequency amplification [15]. Thus, circuits-and-feedback concepts can shed light into how biological systems work. This book has presented circuit models of the heart in Chapter 20, of the neuron in Chapter 15, and of the ear, vocal tract, retina, and neurons in Chapter 23, which allow us to rapidly understand how these systems work. Circuit models are efficient because they are inherently designed to graphically represent interactions between devices in a system in a meaningful way that lead to functional sub-blocks. Such sub-blocks can parse complex systems

Then, Equations (16.35) and (16.36) in Chapter 16 apply exactly to piezoelectric energy harvesters and describe their energy efficiency. From [8], since the mathematics of through-and-across variables is very similar for electromagnetic and electrostatic energy harvesters, we can analyze other motion-energy harvesters through the equations of Chapter 16 as well. Through variables are analogous to generalized current variables while across variables are analogous to generalized voltage variables. Later in this chapter, we shall discuss the operation of electric motors, which are electromagnetic energy generators (harvesters) that operate in reverse. This discussion will further illustrate the similarity between different kinds of electromechanical devices.

In Chapter 16, since we had a required load power consumption in the secondary and we wanted to ensure that the reflected power consumption in the primary due to this load was maximal, we focused on optimizing energy efficiency. In many energy-harvesting situations, energy efficiency may not be as important as maximizing energy transfer, i.e., getting as much absolute energy out of the harvester as possible, even if it means that a large fraction of energy is wasted. For example, in a resistive-divider circuit composed of a voltage source with a source impedance R_S driving a load impedance R_L, energy efficiency is maximized when $R_L \gg R_S$; maximum energy is transferred from the source to the load when $R_L = R_S$, where the energy efficiency is only 50%. In this case, in the terminology of Chapter 16, it can be shown that for maximal power transfer

$$Q_L^{opt} = \frac{Q_2}{1 + k^2 Q_1 Q_2} \tag{26.7}$$

The power dissipated in the electrical load P_e at this optimal value is related to the power dissipated at the mechanical input with no reflected load (d or $k = 0$), P_m, according to

$$\frac{P_e}{P_m} = \frac{1}{4}\left(\frac{k^2 Q_1 Q_2}{k^2 Q_1 Q_2 + 1}\right) \tag{26.8}$$

Piezoelectric harvesters for wireless sensor networks are described in [10] and have generated 180–335 μW in 1 cm^3 of volume. They can be adapted for use in the noninvasive medical-monitoring systems described in Chapter 20. A piezoelectric energy harvester that scavenges energy from compression of the shoe sole has been able to generate 0.8 W of electrical power [11], [12]. Attempts to generate large amounts of electrical power from body motions, however, create a significant reflected electrical load on the mechanical side such that the metabolic effort needed to generate electrical power is consciously felt by the user. Since only 25% of the chemical oxidative energy of glucose is output as useful mechanical work by the body, even a highly efficient energy harvester at 31% can lead to a metabolic load to the body that is 12 times greater than the energy being harvested. One innovative effort to reduce such metabolic loading on the body uses an electromagnetic energy harvester placed on a knee brace slightly above the knee that harvests energy only during leg decelerations. It helps the leg to

the driver and his control strategy of the actuating system, i.e., the car, ensures that the car stops and starts at needed positions along the way, with what is usually adequate precision. Thus, the task, technology, topology, speed, and precision costs of a low-power system illustrated in the low-power hand of Figure 1.1 also apply to cars. The car already implements one good principle of low-power design through its use of a feedback loop, i.e., it separates the costs of speed and precision by having an accurate sensor (the driver's eyes) and control system (the driver's brain) determine the precision of transport while the actuator determines its speed. The mutual information that is of relevance in a transportation task is that between a desired smooth, relatively fast transport trajectory in the head of the driver and the actual transport trajectory that is achieved. In the future, a trajectory that weighs the costs of carbon emissions will also be important.[3]

One principle of low-power design that cars can exploit in the future lies in improving the balance between computation costs and communication costs. Cars can wirelessly communicate with traffic lights and with each other such that the transportation of several drivers is more optimal, therefore saving energy. For example, traffic lights could automatically adapt their timing within a reasonable range such that the directions and locations of high flux have lower waiting times than the directions and locations of lower flux. Traffic lights can be coordinated and synchronized like interacting phase-locked loops that receive correction inputs based on traffic flux counts. Traffic lights could also adapt to patterns that are automatically recognized as being due to an accident scenario. The power costs of wireless transmission for relatively short ranges is extremely cheap, especially when compared with the phenomenal power costs of transportation (1 to 10 W versus tens of kW). Furthermore, energy harvesting from LEDs in traffic lights or RF transmissions from incoming cars can provide constant recharging boosts to such systems such that they can be self-powered (see Chapter 17 for a discussion of far-field wireless recharging systems). Car-to-car hopping can be used for longer-range communication, which is significantly more power efficient per unit distance than a non-hopping strategy ($N(R/N)^2 < R^2$ for $N > 1$ in an N-hop network). Needless to say, the benefits of such sensor-network schemes will have to be weighed against their costs and ease of implementation within an existing infrastructure. Adaptive traffic lights and car-to-car communication are being researched [33].

We shall now shift gears from discussing how to minimize power consumption to discussing how to generate power. We shall begin with what is likely to be the most important source of the power in our future, solar electricity.

[3] Accidents result because of conflicting control algorithms in the heads of different drivers, the imprecision and/or slow reaction times of a drunk-driver's control algorithm, or the disobedience of traffic rules. Thus, driving precision is strongly determined by feedback loops. The power costs of precision are largely borne by the driver and are relatively small. From [27], D. J. Morton and D. D. Fuller. *Human Locomotion and Body Form* (New York, NY: Waverly Press, Inc., 1952), they are estimated to be an additional 83 W over the basal 81 W metabolic rate of the driver.

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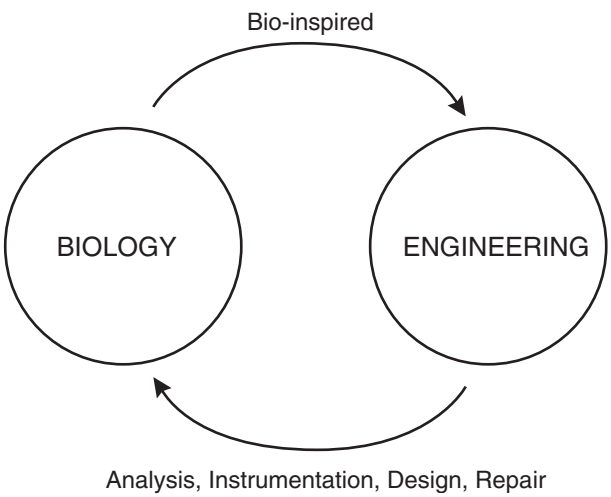
Index

Epilogue

Information is represented by the states of physical devices. It costs energy to transform or maintain the states of these physical devices. Thus, energy and information are deeply linked. It is this deep link that allows us to articulate information-based principles for ultra-low-power design that apply to biology or to electronics, to analog or to digital systems, to electrical or to non-electrical systems, at small scales or at large scales. The graphical languages of circuits and feedback serve as powerful unifying tools to understand or to design low-power systems that range from molecular networks in cells to biomedical implants in the brain to energy-efficient cars.

A vision that this book has attempted to paint in the context of the fields of ultra-low-power electronics and bioelectronics is shown in the figure below. Engineering can aid biology through analysis, instrumentation, design, and repair (medicine). Biology can aid engineering through bio-inspired design. The positive-feedback loop created by this two-way interaction can amplify and speed progress in both disciplines and shed insight into both. It is my hope that this book will bring appreciation to the beauty, art, and practicality of such synergy and that it will inspire the building of more connections in one or both directions in the future.



Epilogue The two-way flow between biology and engineering.