

input sequence	register contents				output sequence
$s_5s_4s_3s_2s_1 \rightarrow$	t_1	t_2	t_3	t_4	$\rightarrow x_2(5)x_2(4)x_2(3)x_2(2)x_2(1)$
00101	0	0	0	0	
0010	1	0	0	0	1
001	1	1	0	0	11
00	1	1	1	0	111
0	1	1	1	1	1111
	0	1	1	1	11111