Problems for Chapter 9 of 'Ultra Low Power Bioelectronics'

Problem 9.1

A 'final-value theorem' in linear systems states that the final value of the output $Y(s)$ of a linear system with transfer function $H(s)$ to an input $X(s)$ is given by

$$\lim_{t\to\infty}\{y(t)\}=\lim_{s\to 0}\{sY(s)\}=\lim_{s\to 0}\{sH(s)X(s)\}$$

The error $\varepsilon(s)$ in a negative-feedback system is given by

$$\varepsilon(s)=\frac{1}{1+L(s)}$$

a) Show that if a negative-feedback loop transmission is to have zero steady-state error in response to a *step input*, $L(s)$ as $s\to 0$ must scale at least as fast as $1/s$ ($1/s^n$ with $n > 1$). Thus, if a phase-locked loop is designed to track input phase, *zero steady-state phase error* implies that the loop transmission near the origin in this loop must scale at least as fast as that of a first-order integrator.

b) Show that if a negative-feedback loop transmission is to have zero steady-state error in response to a *ramp input*, $L(s)$ as $s\to 0$ must scale at least as fast as $1/s^2$ ($1/s^n$ with $n > 2$). Thus, if a phase-locked loop is designed to track input frequency, *zero steady-state frequency error* implies that the loop transmission near the origin in this loop must scale at least as fast as that of a second-order integrator.

Problem 9.2

For the loop transmission $L(s)=\dfrac{1}{(s+1)(0.1s+1)(0.01s+1)}$:

a) Plot the gain, $|L(j\omega)|$, and phase, $\angle L(j\omega)$, Bode plots. All asymptotes, important values, and locations of important values should be indicated on the plots.

b) On the $L(s)$ Nyquist plane, plot $L(s)$ as s traverses various regions of the right half plane D contour. Why is the plot symmetric about the x-axis?

c) For K positive, find the value of K at which the closed loop system with loop transmission $KL(s)$ just goes unstable. When it is unstable, how many unstable poles does the system have? Show how the Nyquist plot for the system makes the same prediction as the root-locus plot.

d) Repeat part c) for K negative (find $|K|$ for which the system goes unstable.)

Problem 9.3

Several sensorimotor feedback loops (e.g. brain control of the hand via the eye) in neurobiology and molecular feedback loops in cell biology (e.g., the up-regulation or down-regulation of protein concentration in response to environmental changes) have significant delays within them. Several feedback loops in communication networks have significant delays within them as well.

a) Using a Nyquist plot, show that $L(s)=Ke^{-sT}$, a representation of a loop transmission with a delay of T, is unstable for $|K| > 1$, i.e., if the strength of

the negative-feedback (K is positive) or positive-feedback magnitude (K is negative) of the loop transmission exceeds 1.

b) Find the value of K for which $L(s) = (K/s)e^{-sT}$ has a phase margin of 45^0 under negative feedback (K is positive). Your answer should be expressed in terms of T.

Problem 9.4

The circuit shown below consists of two transistors with their bulk connected to ground. Transistor M_1 is biased at a dc gate voltage of V_{BIAS}, and establishes the dccurrent for both transistors. M_2 is biased at a dc gate voltage of V_{CASC}, which establishes the drain voltage of M_1. M_2 is called a cascoding transistor. A dc current flows through the two transistors, but its value is not important for this problem. Also, where the drain of M_2 connects to is not important for this problem. What we wish to characterize is the small-signal, dc output resistance of this cascoded NMOS structure. It can be shown through nodal analysis that the equation for the small-signal r_{out} is:

$$r_{out} = r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o1}r_{o2}$$

where r_{ox} is transistor M_x's small-signal output resistance, and g_{m2} and g_{mb2} are the small-signal gate and bulk transconductances of M_2.

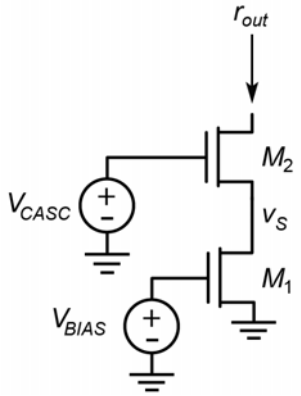

Figure P9.4 Cascoded transistor.

We can rewrite the r_{out} equation as:

$$r_{out} = (r_{o1} + r_{o2})[1 + (g_{m2} + g_{mb2})(r_{o1} \| r_{o2})]$$

This suggests that the impedance (r_{o1}+r_{o2}) is effectively increased by a factor of (1+A) where $A = (g_{m2}+g_{mb2})(r_{o1} \| r_{o2})$ is the loop gain of a feedback loop. We will explore this feedback viewpoint in this problem.

a) Draw the complete small-signal dc model of this transistor pair.

b) Apply a small-signal test voltage v_{test} at the drain of M_2 in your small-signal model from part a). Using nodal analysis, solve for i_{test}, the resulting drain current of M_2, and use this to confirm the above equation for r_{out}.

c) Now, use the fake-label technique to draw a block diagram of the feedback loop which increases r_{out}: First, using superposition, express v_s as a function of the test voltage v_{test} and the fakely independent current source in M_2; then, introduce the dependence of the current source on v_s to create a feedback loop.

d) Find i_{test} as a function of v_s.
e) Draw a feedback block diagram that illustrates that the dependent generator of M_2 attenuates the feed-forward transfer function from v_{test} to v_s and thus the transfer function from v_{test} to i_{test}. Using Black's formula, find the transfer function from v_{test} to i_{test} and hence show how r_{out} can be expressed in terms of the loop gain A, r_{o1} , and r_{o2}.

Problem 9.5

A Schmitt trigger and an integrator are hooked to one another in a negative-feedback loop (one system's output to the other's input and vice versa) to create an oscillator. Such relaxation oscillators are common in nature (Sodium-Potassium action potential generation in the nervous system and cellular circadian rhythyms) and also in engineering (function generators).

a) For the system to oscillate, it must be unstable. Explain why, at the onset of instability or oscillation, the negative-feedback loop transmission has a magnitude of 1 and a phase of -180^0.
b) The nonlinear Schmitt trigger is well described by the describing function given in Equation (9.17) while the linear integrator is well described by the transfer function $(1/\tau s)$. From these facts, argue that the amplitude of sinusoidal oscillation at the input of the Schmitt trigger must be E_S.
c) Find the frequency of oscillation in terms of τ and the parameters of Equation (9.17).
d) Explain physically why the oscillation is stable at only one particular amplitude.
e) Explain physically why the oscillation is stable at only one particular frequency.
f) The circuit of Figure P9.5 implements a system similar but not identical to that discussed in the problem thus far. Explain intuitively how it works assuming that the output of the operational-amplifier-based Schmitt trigger oscillates between +15 V and -15 V.
g) From your knowledge of RC-circuit responses to square waves and the trip points of the Schmitt trigger compute the frequency of oscillation of Figure P9.5.

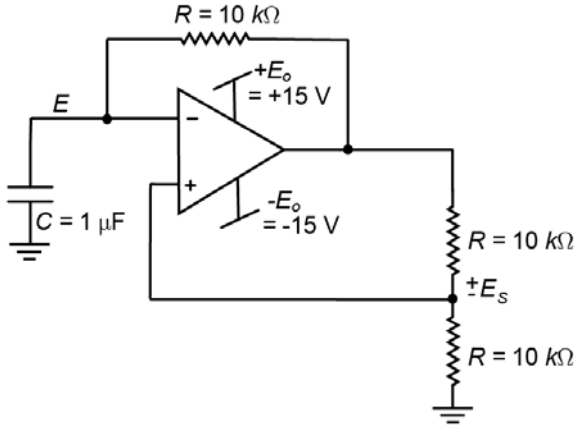

Figure P9.5 A relaxation oscillator with positive and negative feedback.

Problem 9.6

An example of a negative-feedback loop transmission in certain high-order phase-locked loops (described in Chapter 18) and sigma-delta analog-to-digital converters (described in Chapter 15) is well described by

$$L(s) = K\frac{(10^{-6}s+1)^2}{(10^{-5}s)^3}\frac{1}{(10^{-8}s+1)^2}$$

a) Draw Bode plots of the gain ($L(j\omega)$) and phase ($\measuredangle L(j\omega)$) of $L(s)$ for K=1.

b) From your Bode plots or a Nyquist plot, predict the minimum value of $K > 0$ at which the closed-loop system is stable.

c) From your Bode plots or a Nyquist plot, predict the maximum value of $K > 0$ at which the closed-loop system is stable.

d) Draw a root-locus plot that illustrates how the closed-loop poles vary as K varies from 0 to ∞. Are your results from parts b) and c) consistent with the root-locus plot?

Problem 9.7

Answer the following questions about the OTA-C circuit shown in Figure P9.7

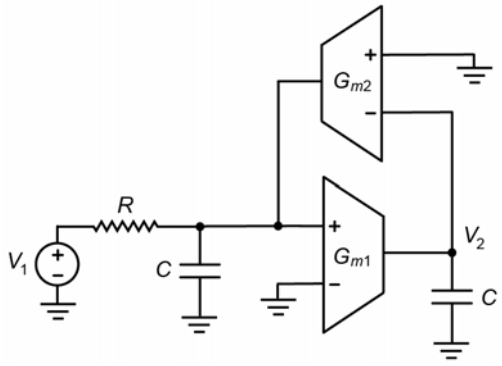

Figure P9.7 OTA-C

a) Draw a block diagram that relates V_1 to V_2 in terms of the circuit parameters. The trapezoidal blocks represent ideal transconductors with output currents proportional to their differential input voltages and infinite output impedance.

b) Using your block diagram, compute the transfer function $\frac{V_2(s)}{V_1(s)}$. Write your answers in a canonical form as shown below. Make sure you define τ and Q in terms of the parameters given.

$$\frac{V_2(s)}{V_1(s)} = \frac{A_{cl}}{\tau^2 s^2 + \frac{\tau s}{Q} + 1}$$

c) Show that your answers to τ and Q in part b) are consistent with the closed-loop τ-and-Q rules of Equation (9.16).

d) Sketch the root locus of your loop transmission as G_{m2} is varied from 0 to infinity. Label the open-loop pole locations and any real-axis entry/breakpoints of the root locus.

e) If $G_{m1} = G_{m2} = 1$ μA/V, and $C = 10$ pF, find the value of R such that $Q = \frac{\sqrt{2}}{2}$.

Problem 9.8

Figures P9.8 (a) and P9.8 (b) show a simple gain-of-100 current mirror and a more complex gain-of-100 current mirror with $(W/L)_{M1} = 1$, $(W/L)_{M3} = 1$, $(W/L)_{M4} = 1$, $(W/L)_{M2} = 100$, and $(W/L)_{M5} = 100$. The length $L = 6$ μm in all devices. For this problem, assume that all Early voltages are infinite, $\kappa = 0.7$, and $C_{ox} = 10^{-3}$ F/m^2.

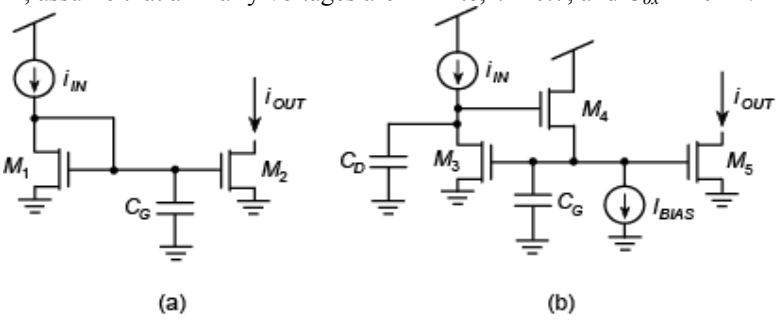

Figure P9.8 A simple current mirror in (a) and a more complex current mirror in (b).

a) Assuming that all capacitances shown in the circuit above are due to intrinsic capacitances present in the MOS transistors, that all transistors are in subthreshold, and that the current mirrors are ideal with infinite impedance, evaluate C_G in (a) and C_G and C_D in (b). (Hint: Use Equation (5.48) and the transistor dimensions.)

b) Find the transfer function $\frac{I_{out}(s)}{I_{in}(s)}$ in terms of C_G and the small-signal parameters of M_1 and M_2 for Figure P9.8 (a). The circuit's transfer function can be represented by a low-pass response $\frac{100}{1+\tau_1 s}$. Compute the time constant τ_1 in terms of these same parameters

c) Draw a small-signal model for the circuit of Figure P9.8 (b), derive a block diagram, and compute the loop transmission $L(s)$ of the feedback loop formed by M_4 and M_3.

d) For the values found in part c), draw a Bode gain and phase plot of the loop transmission, $L(s)$, when $i_{IN} = 1$ nA and $I_{BIAS} = 70.7$ nA from 10 Hz to 10 MHz. Label all slopes, the unity-gain frequency, all breakpoints, and compute the phase margin.

e) Is the closed-loop relationship between $I_{in}(s)$ and $I_{out}(s)$ in Figure P9.8 (b) consistent with Equation (9.16) and also with Equation (9.8)?

f) If I_{BIAS} is greater than 10,000I_{IN}, explain why the circuit of Figure P9.8 (b) can be well approximated by a lowpass filter with a time constant $\tau_2 = \frac{C_D I_{IN}}{\kappa \phi_t}$. In this situation, and if I_{IN} is the same in the circuits of Figure P9.8 (a) and P9.8 (b), how much larger is the bandwidth of the circuit of Figure P9.8 (b) than the bandwidth of the circuit of Figure P9.8 (a)?

Problem 9.9

For the reduced-gain (Figure 9.9 (b)), lag (Figure 9.11(b)), and lead (Figure 9.12 (b)) compensation topologies, compute for each topology

a) The loop transmission in terms of the circuit parameters of these figures (Use C for the 'High-f capacitor' of Figure 9.12(b)).
b) The ideal closed-loop transfer function from $V_{in}(s)$ to $V_{out}(s)$ assuming that $|L(s)/(L(s)+1)|$ is very near 1.
c) Why is the lead-compensation topology the only compensation topology of the three where the dynamic parameters (settling time, overshoot, rise time) of the closed-loop transfer function from $V_{in}(s)$ to $V_{out}(s)$ are not solely determined by the $L(s)/(L(s)+1)$ transfer function?

Problem 9.10

This problem requires the use of a circuit simulator such as SPICE. In this problem we will study how to stabilize a three-stage op-amp, shown in Figure P9.10, using minor-loop compensation. Use the following parameters in this problem: $W_1 = W_9 = W_{11} = 3.6\ \mu$m, $W_2 = W_7 = W_8 = 14.4\ \mu$m, $W_3 = W_4 = 18\ \mu$m, $W_5 = W_6 = W_{10} = 7.2\ \mu$m, the length of all transistors is 3.6 μm, $I_{REF1} = 125$ nA, $I_{REF2} = 4.5\ \mu$A, $R_L = 630$ kΩ, $V_{BIAS} = 1.33$ V, and $V_{DD} = 5$ V.

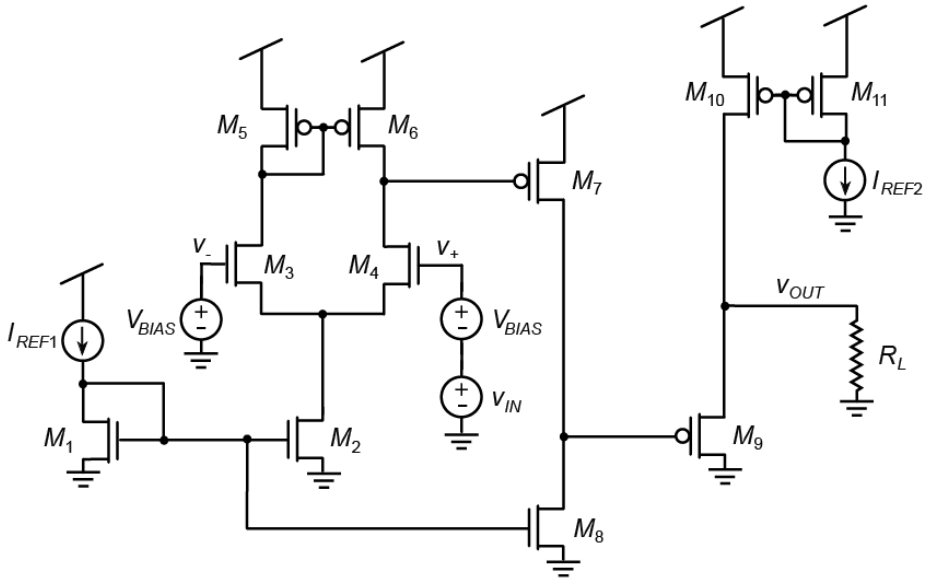

Figure P9.10 Three-stage op-amp.

a) Plot the gain and phase of $V_{out}(s)/V_{in}(s)$. Is the op-amp stable under unity feedback? Determine the location of the first two poles.

b) In order to stabilize the operational-amplifier when it is used in feedback configurations, we shall exploit minor-loop compensation: we place a resistor in series with a capacitor between the gate and drain of M_7. The resistor cancels the RHP zero created by the feedforward path through the capacitor while the capacitor serves the minor-loop function described in the text. Determine the capacitor and resistor values that are needed to obtain 45º of phase margin when the op-amp is used in a unity-gain feedback configuration (buffer). Provide a schematic and a plot of the gain and phase characteristics of the operational amplifier.